KeyASIC

Package Strategy, Package Design & Good Practice

March 2019

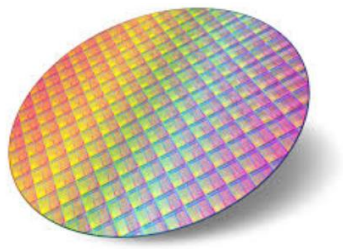
Moscow

Backend Services

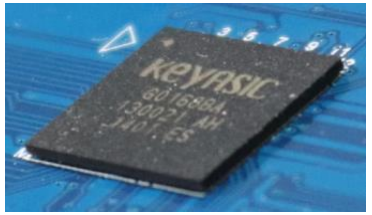
PW: FE, IP
PRF: BE
Area: INTG VRFY, TEST
Cost: PKG

Manage, Control & Overlook

Wafer

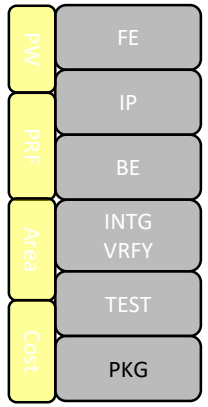


Packaging



Testing

Packaging Services



- Co-design & develop IC packaging with assembly partners

- IC Packaging documentation

- Package qualification

- Improve on packaging & yield

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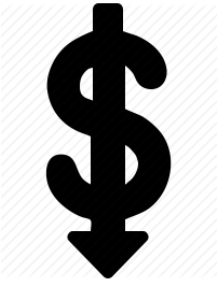
Objective

PW
PRF
Area
Cost

FE
IP
BE
INTG
VRFY
TEST
PKG



Reduce Overall Cost

Enhance Performance

Manufacturability of Final Design

Time to Market

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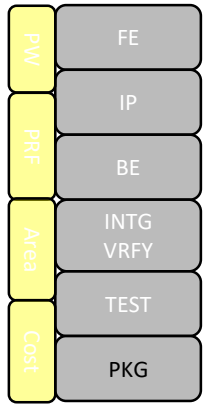
Packaging Strategy



- Package Requirement
- Known Good Dies (KGDs)
- Application Specific IC’s (ASICs)
- Advance in Substrate Technology
- Working Together

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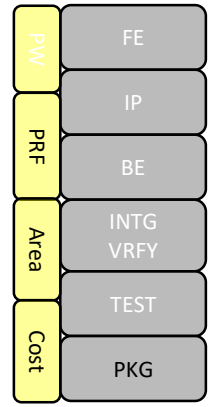
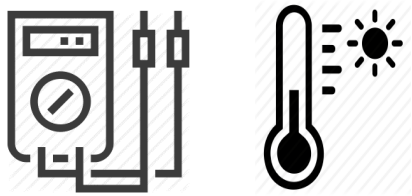
Packaging Strategy

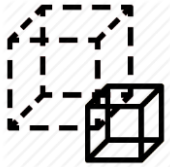


Package Requirement

- Thermal & Electrical Requirement

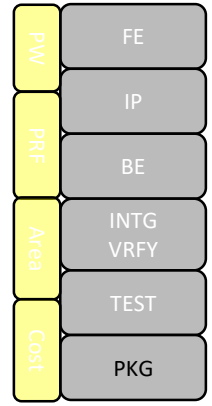


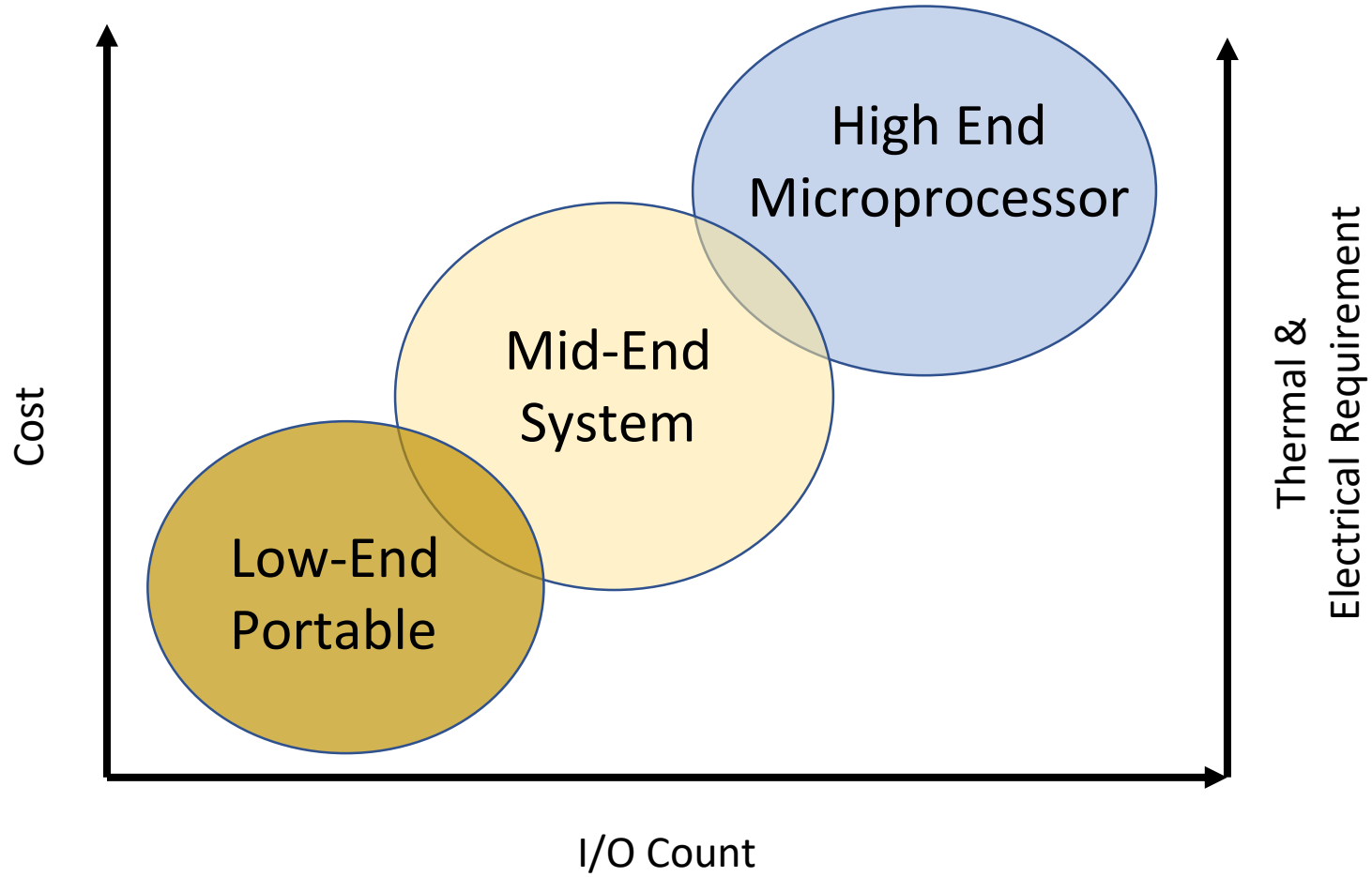
- Real-Estate Constraint



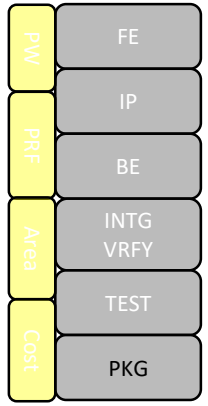
- Cost

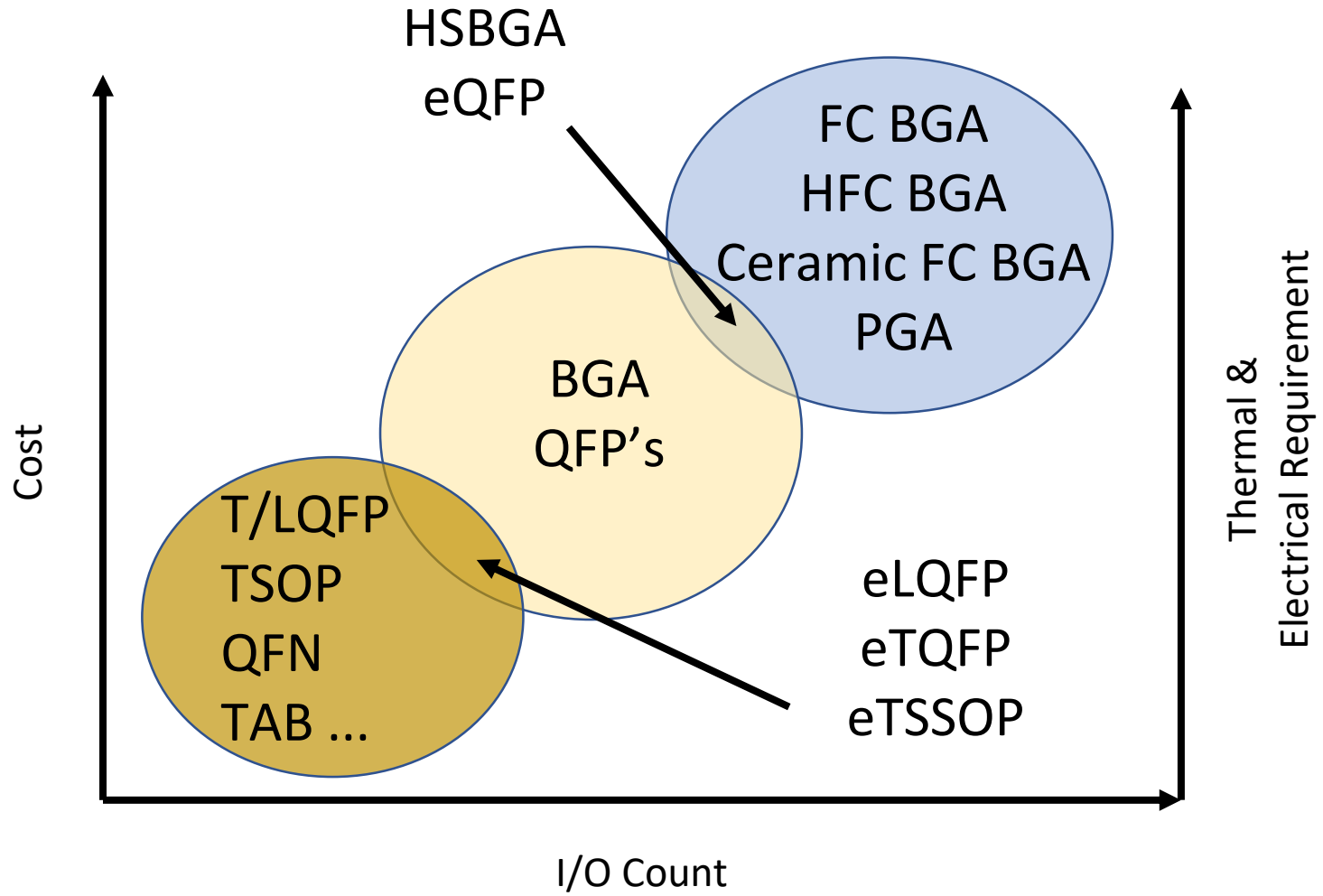
Packaging Strategy





Packaging Strategy

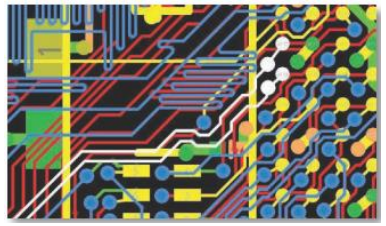


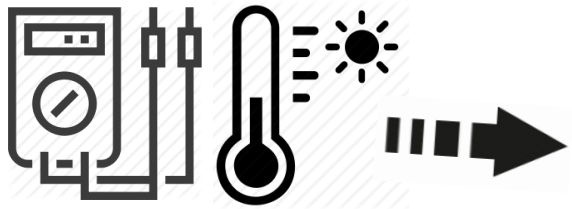


Packaging Strategy

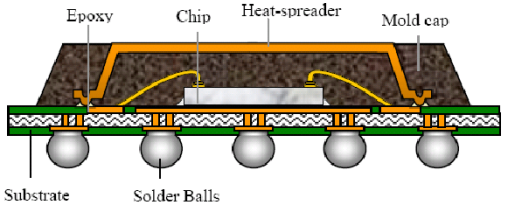
Electrical & Thermal Enhancement

Capacitance Control Features

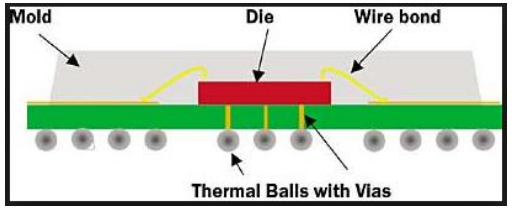




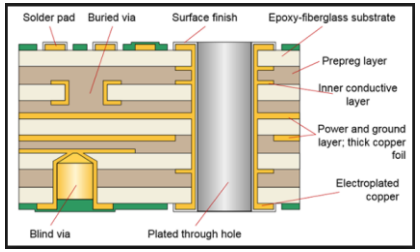
Heat Spreader



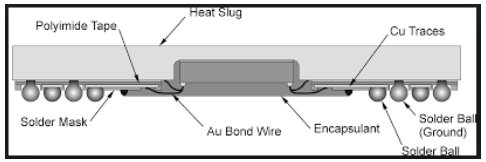
Thermal Vias



Multilayer substrates



Heat Slugs



PW
PRF
Area
Cost

FE
IP
BE
INTG VRFY
TEST
PKG

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Packaging Strategy

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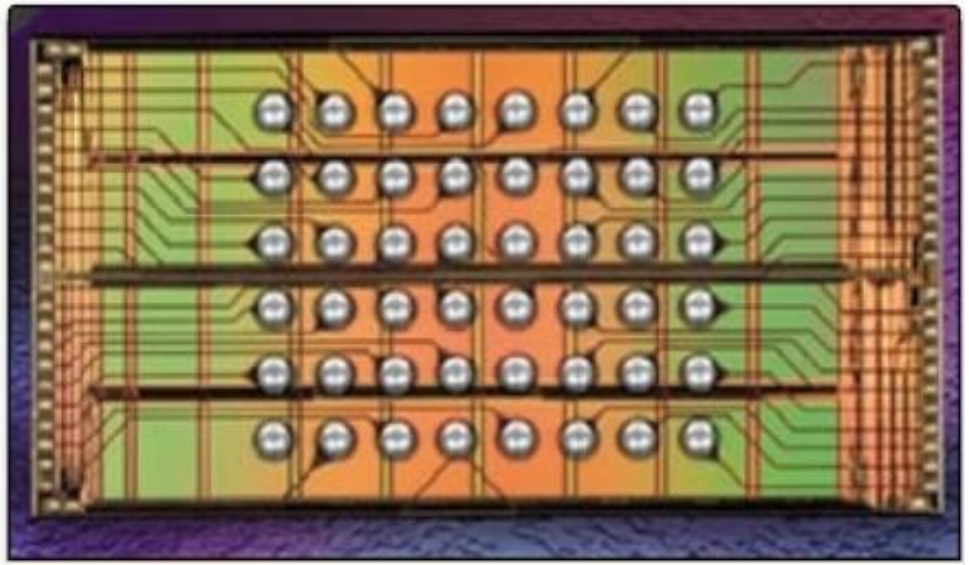
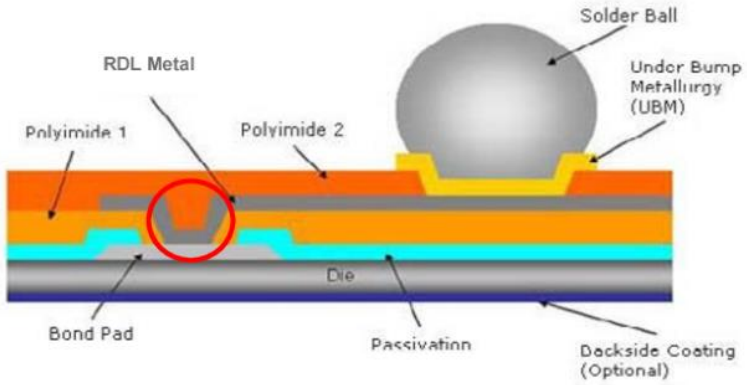
Known Good Dies (KGDs)

- Easily converted to an array format
- Re-distribution layer (RDL)





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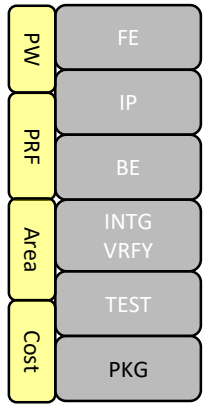
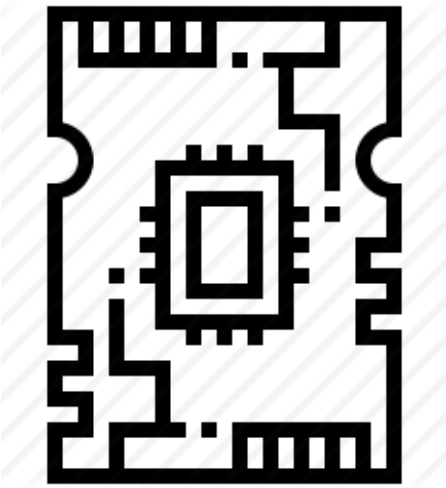
Packaging Strategy



Application Specific IC's (ASICs)

- Higher level of circuity
- Chip-to-substrate interconnect level
- Thermal management solution



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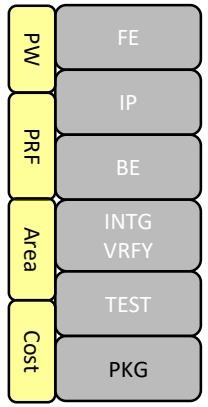
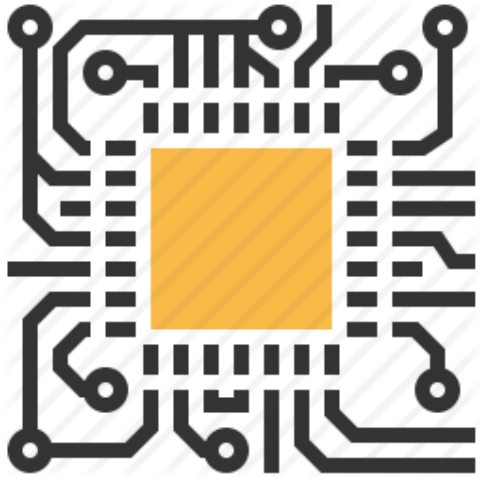
Packaging Strategy

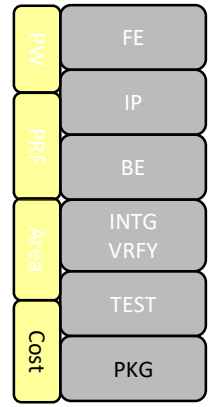


Advance in Substrate Technology

- Need for more I/O's and smaller ball pitches
- Through & blind vias
- Plating tail & gold plating process



Packaging Strategy



Working Together

- Utilization of standard tools and documentation

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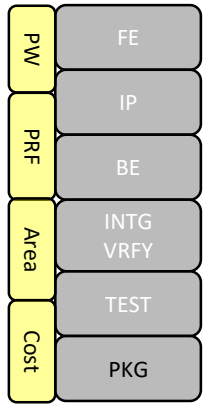
Packaging Flow



Traditional Design Flow

Early planning

Power-Ground-I/O Planning & Physical Synthesis

Si Closure Routing & Finishing

IC Flow

To Wafer Tape out

Netlist
Constraints
I/O Drivers
.....

Substrate Pattern & Routing Layout

Design Verification & Optimization

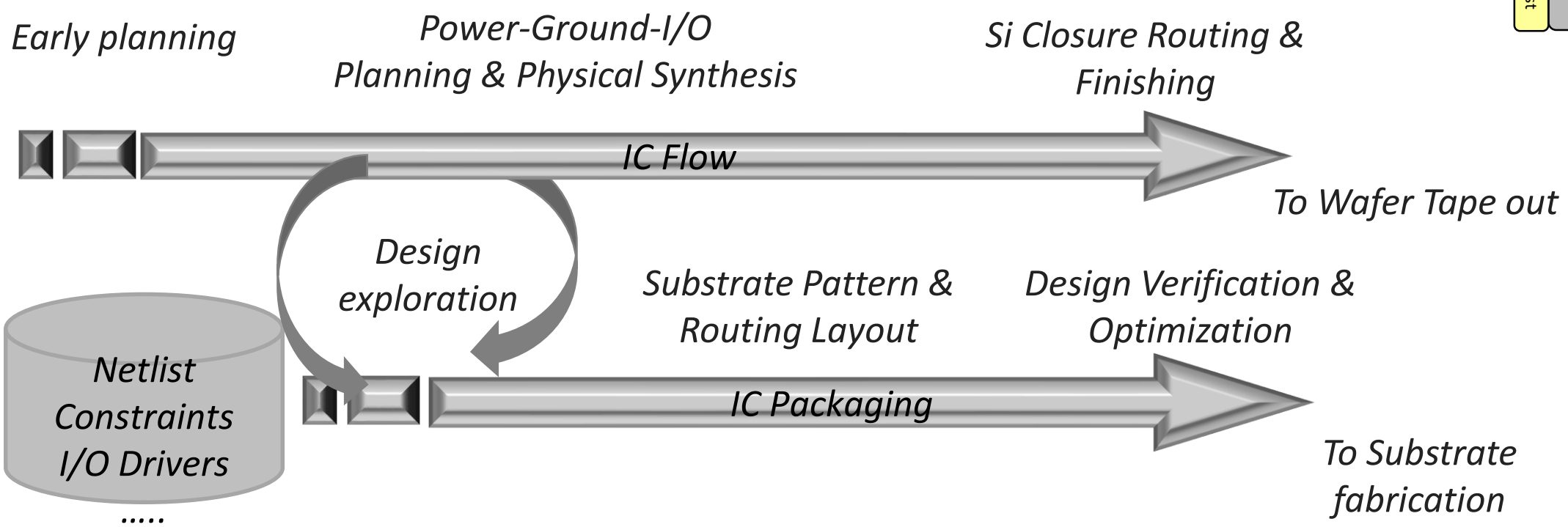
IC Packaging

To Substrate fabrication

Packaging Flow

PW | FE
PRF | IP, BE
Area | INTG VRFY
Cost | TEST, PKG

Design Convergence (Co-Design) Flow



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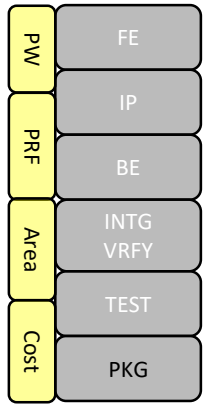
Packaging Flow



Design Convergence (Co-Design) Flow

Why packaging involvement at early planning?

E.g.

Competitor Price in Market USD2.00

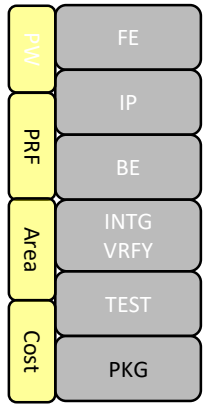
Target to price compete in Market USD1.00

Unit Price Breakdown (est)

- Die	40%
- Assembly	30% (USD0.30)
- Testing	10%
- Margin & GA	20%

- Find a package (type, lead/ball count) within this cost or lower
- Work with IC Design to work within this package (type, lead/ball count)

Package Selection by Design



- Thermal Performance
- Electrical Performance
- Physical Consideration
- Package Connectivity
- Manufacturing Consideration

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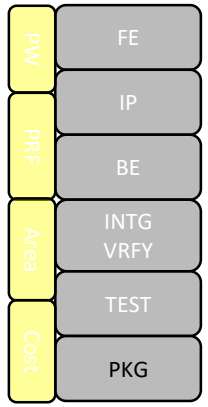
Package Selection by Design



Preliminary Information (Estimation)

- Die Size
- I/O Count (chip & package)
- Thermal Dissipation & Electrical requirement
- End User Application & Environment
- Cost
- Time to Market

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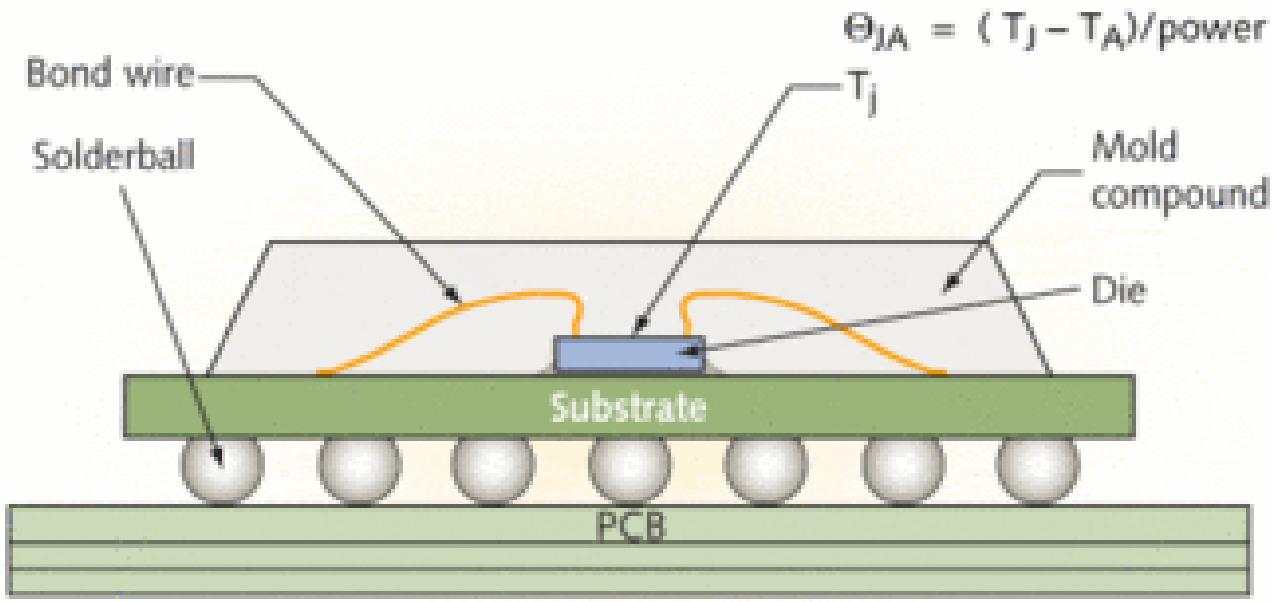
Package Selection by Design

PW | PRF | Area | Cost

FE
IP
BE
INTG VRFY
TEST
PKG

Thermal Performance is Primary!



T_J = Maximum junction temperature

T_A = Ambient temperature inside the chamber

Power = The amount of power, measured in watts produced by the device

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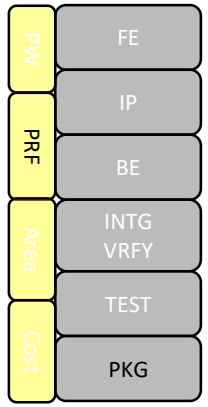
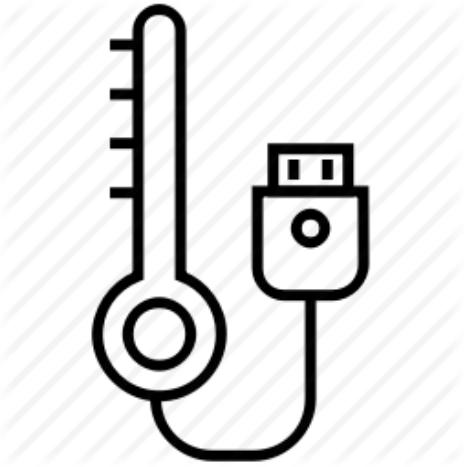
Package Selection by Design



Thermal Performance Solutions

- Exposed Die Attach Pad (DAP)
- Increase Substrate Layer Count
- Substrate Copper Plane Thickness
- Heat Sink or Slugs
- Substrate Filled Vias
- Thermal Balls
- Increase Package Size



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Package Selection by Design

Thermal								Theta JA (Deg C/W)		
Package	Ball/Lead count	Pkg Size (mm)	Pad size (mil)	Die Size (mil)	Heatspreader /Heatsink	LF/Substrate Material	PCB Layer	0 (m/s)	1 (m/s)	2 (m/s)
QFP	80	14x20	240x240	100x100	-	Cu	4L	26.2	21.3	18.5
QFP	208	28x28	405x405	100x100	-	Cu	4L	37	35.9	34.1
QFP	208	28x28	405x405	400x400	Y	Cu	4L	15.5	13.4	12.2
LQFP	100	14x14	276x276	200x200	-	Cu	4L	39.7	37.7	35.4
LQFP	100	14x14	354x354	200x200	-	Cu	4L	29.9	27.3	25.3
TQFP	100	14x14	240x240	200x200	-	Cu	4L	37.9	34.6	32.8
TQFP	100	14x14	354x354	200x200	-	Cu	4L	32.5	30.2	28.2

Source: ASE

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Package Selection by Design

Thermal							Theta JA (Deg C/W)		
Package	Ball/Lead count	Pkg Size (mm)	Pad size (mil)	Die Size (mil)	Heat spreader/Heatsink	LF/Substrate Material	0 (m/s)	1 (m/s)	2 (m/s)
PBGA	313	35x35	395x395	350x350	-	2L	23.2	20.8	19
PBGA	313	35x35	395x395	350x350	-	4L	19	17.1	15.7
PBGA	569	40x40	486x486	450x450	-	2L	20.5	18.4	16.8
PBGA	569	40x40	486x486	450x450	-	4L	16.5	14.8	13.6
HSBGA	388	35x35	528x528	400x400	Y (36 thermal ball)	2L	16.6	14.7	13.5
HSBGA	388	35x35	528x528	400x400	Y (36 thermal ball)	4L	12.3	10.6	9.3
HSBGA	452	35x35	528x528	300x300	Y (100 thermal ball)	4L	12.8	11.1	9.9

Source: ASE

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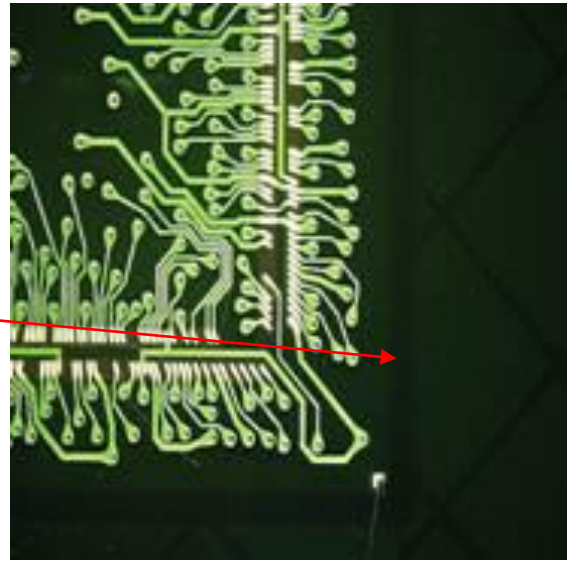
Package Selection by Design

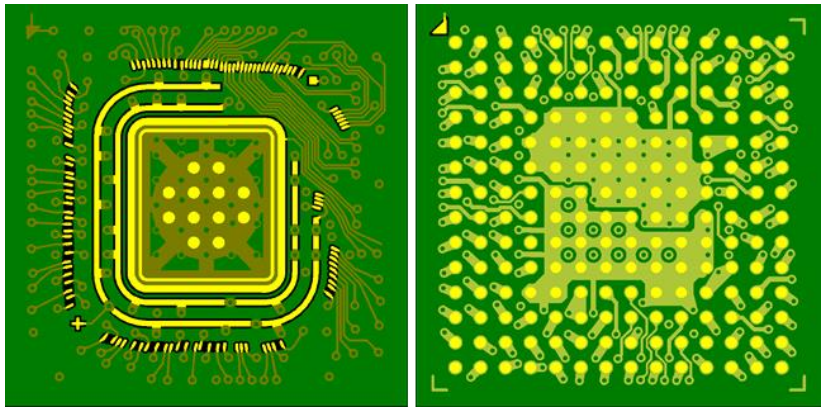
Electrical Performance

- Identifying Critical Signals
- Signal Integrity
- Substrate Plating Requirements
- Substrate or Lead Frame Connectivity

GPP Product

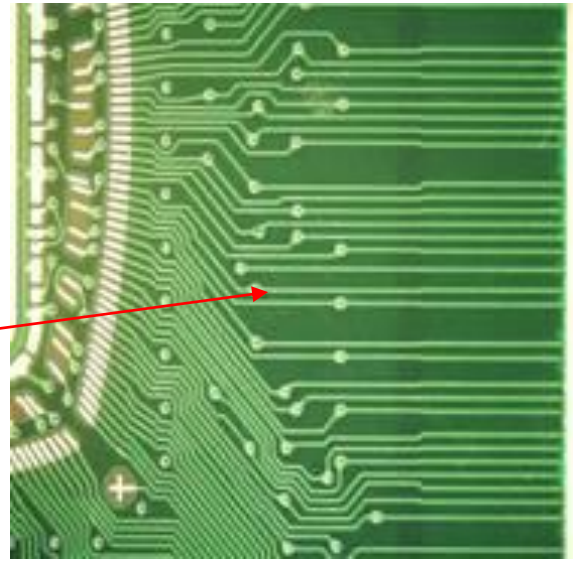
No Tie Bar

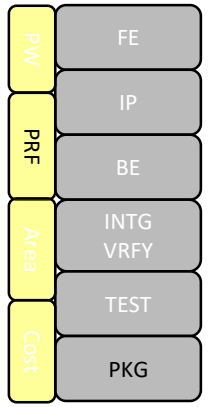




Subtractive Product

Tie Bar





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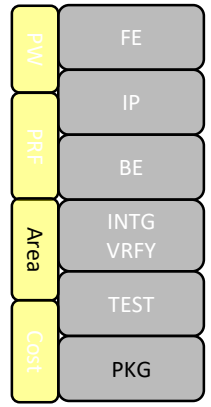
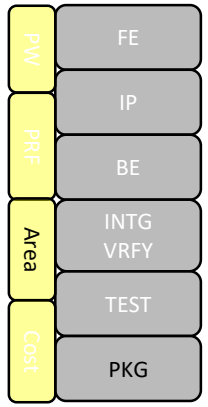
Package Selection by Design



Physical Consideration

- Basic physical package attributes
- Cost considerations
  - Typically custom and tooling availability
- Tester and test socket availability
- PCB connectivity challenges

Package Selection by Design



Package Connectivity

- Interconnects between die pads and lead frame leads/BGA ball locations
- Power and ground rings vs. down bonding to the package DAP
- Standard netlist formats reduces design cycle time

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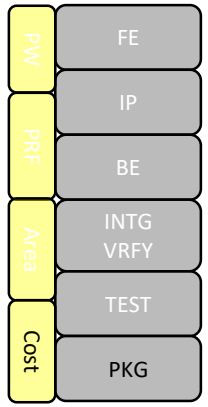
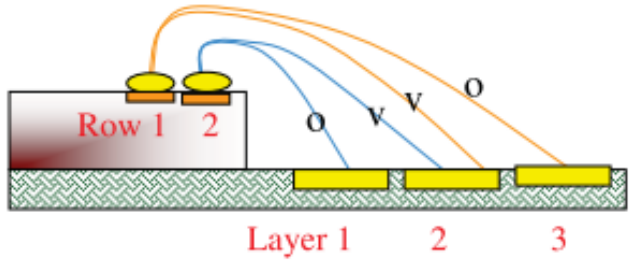
Package Selection by Design



Manufacturing Consideration

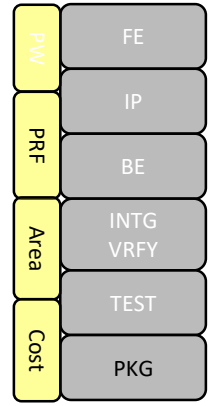
- I/O density with respect to the die size
- Wire lengths
- Wire angles
- Wire loop profiles
- Die pad design
- Lead frame & substrate design features clearances

Max. Wire Length Forward Looping	Wire Diamete
30mil(762um)≦WL≦130 mil(3302um)	18um(0.7mil
30mil(762um)≦WL≦140 mil(3556um)	20um(0.8mil



KeyASIC

Case Study



Single Substrate Design with Multi SDRAM and Flash Options

SDRAM
(est. USD4.50)

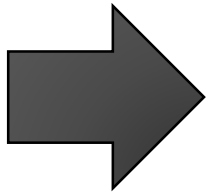
+

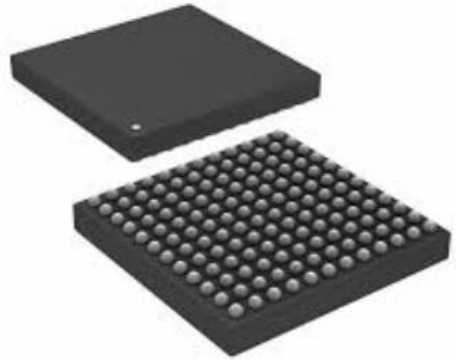
ASIC
eLQFP 28x28 256L
(est. USD1.95)

+

Flash Memory
(est USD2.00)

3 Packages cost (est. USD8.50);
ASIC, SDRAM & Flash





1 package; VFBGA
10x10x0.9mm 144L MCM (est.
USD4.00)

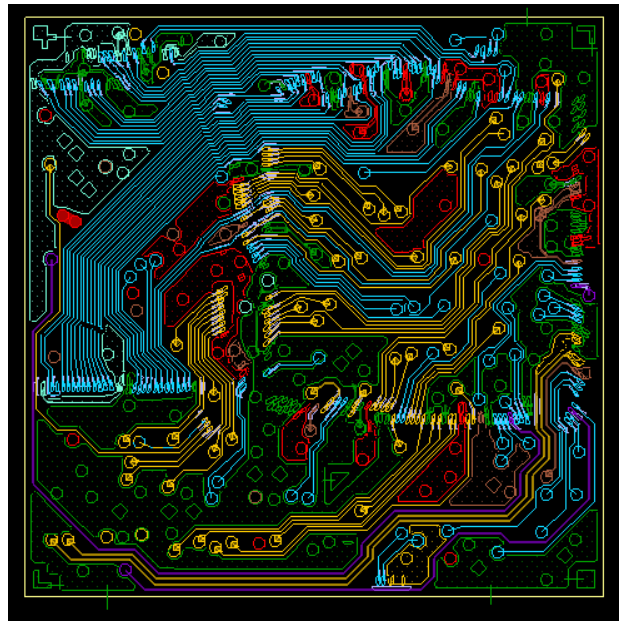
Case Study

PW | PRF | Area | Cost

FE | IP | BE | INTG VRFY | TEST | PKG

Single Substrate Design with Multi SDRAM and Flash Options

ASIC	SDRAM	Flash
KA0268	256MB	32MB
	64MB	64MB



4 in 1 Combo

KeyASIC

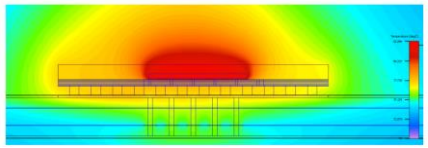
Case Study

PW | PRF | Area | Cost

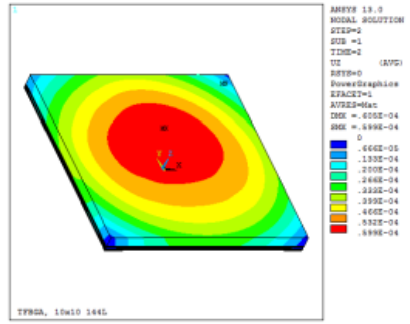
FE | IP | BE | INTG VRFY | TEST | PKG

Challenges:

- Thermal Performance
  - To meet the thermal requirement



- Electrical Performance
  - To meets the electrical performance and timing



Package at 260°C (warpage: +59.9 um)

- Physical Consideration
  - Fitting into real estate constraint of the system

KeyASIC

Case Study

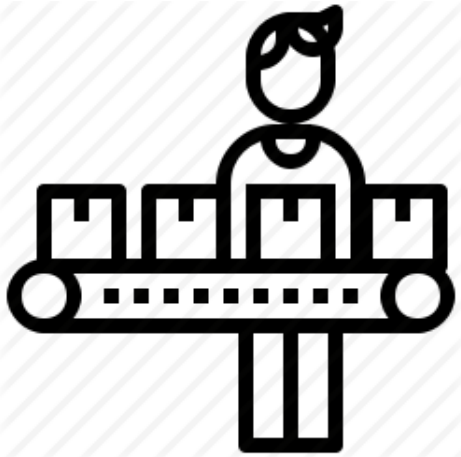
PW | PRF | Area | Cost

FE | IP | BE | INTG VRFY | TEST | PKG

Challenges:

- Package Connectivity
  - Side by side or stacked?

- Manufacturing Consideration
  - Manufacturable in mass production

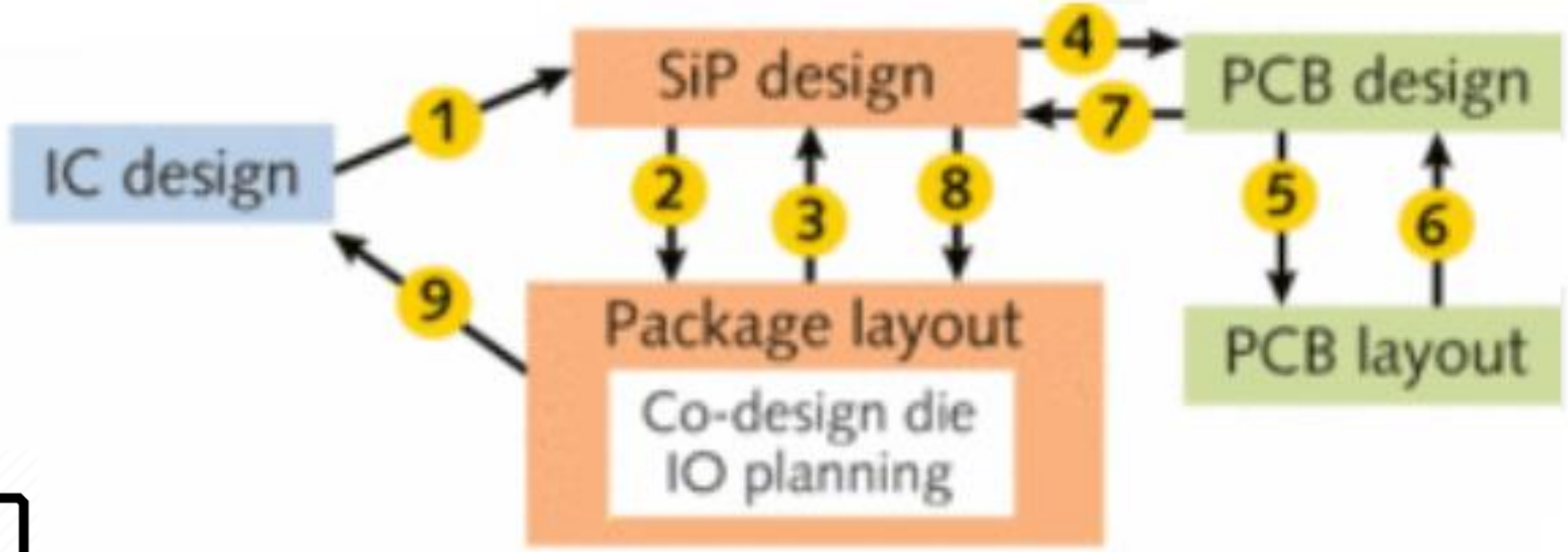


Summary

PW | PRF | Area | Cost

FE | IP | BE | INTG VRFY | TEST | PKG

Working Together: IC / Package / PCB Co-Design Process



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Thank you