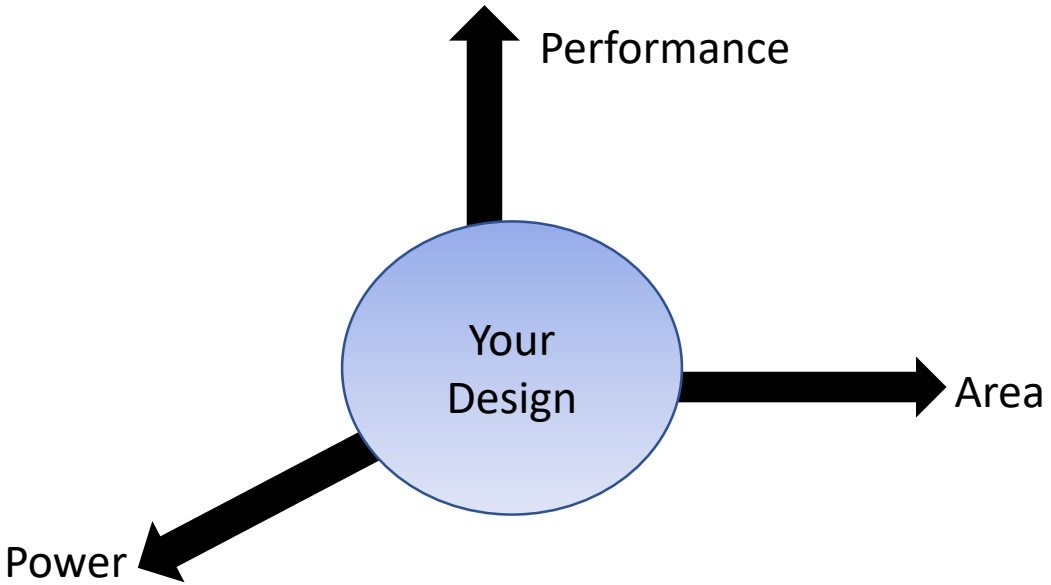
KeyASIC

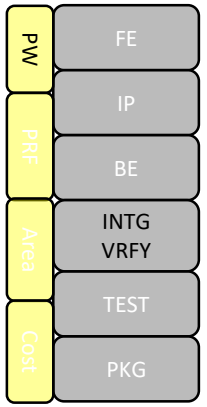
Front end design methodology. Synthesis, timing closure

March 2019

Moscow

PPA space





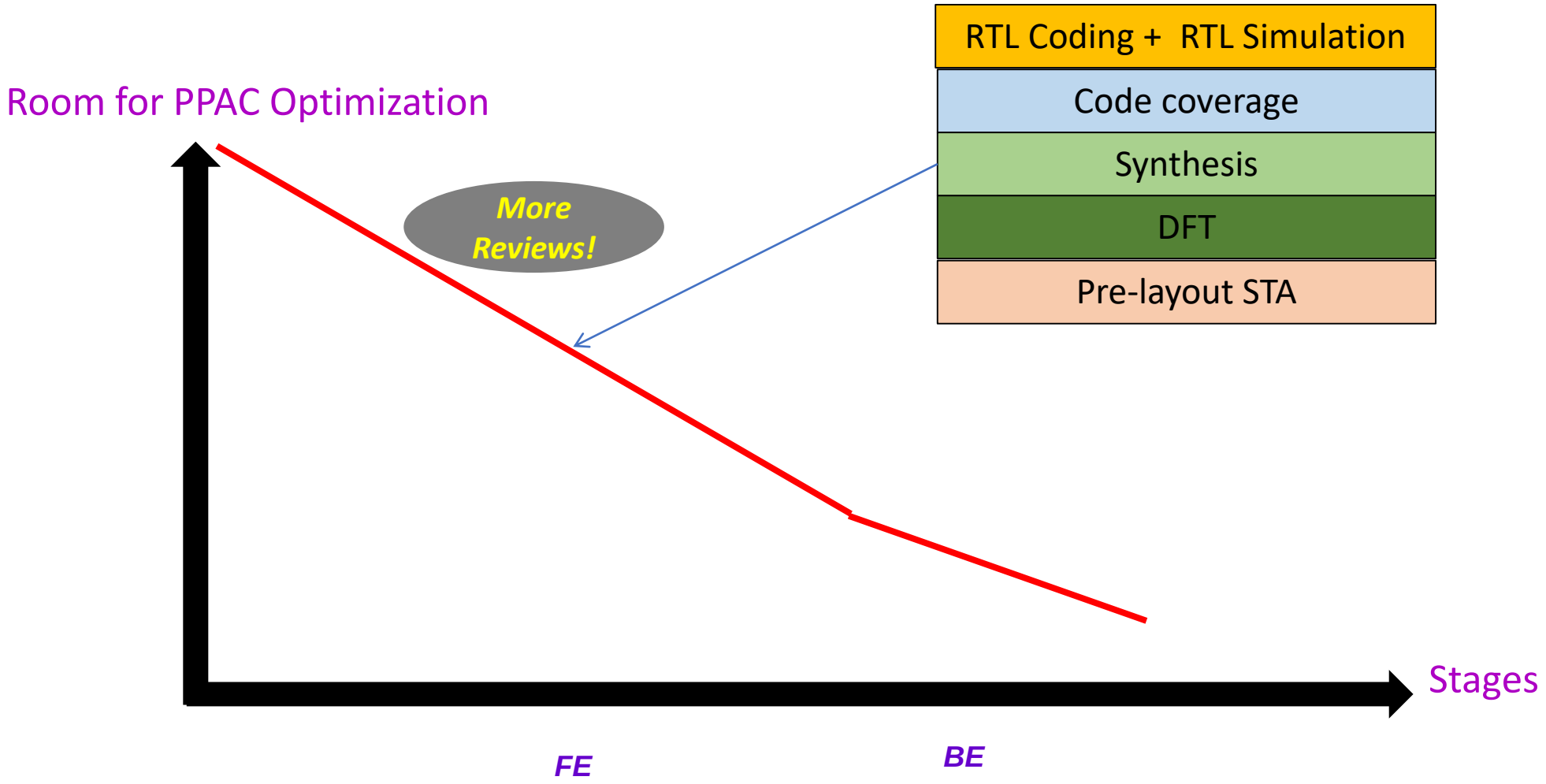
Besides on your spec to balanced PPA space.

EX: You want design the max Power .

In the FE begin, you need consider in mind for Power

KeyASIC

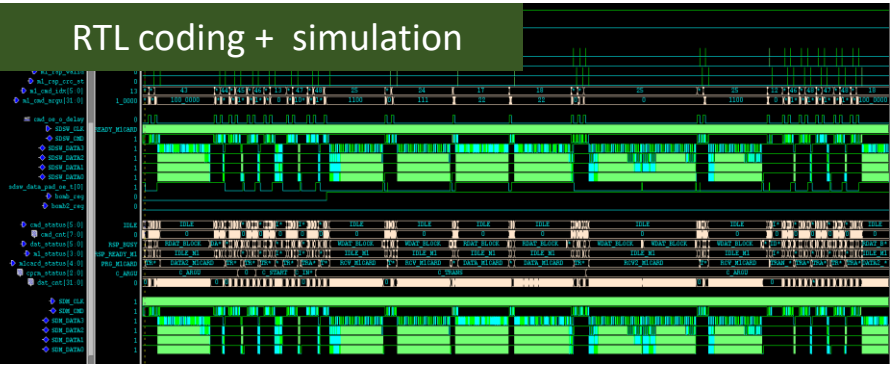
FE design with PPA space



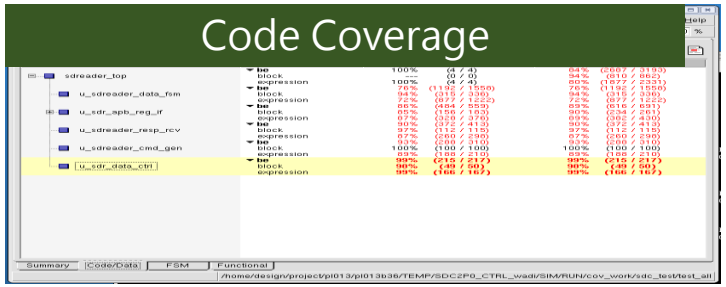
KeyASIC

FE

RTL coding + simulation



Code Coverage



Synthesis

- Check constrain is meet spec
- Good constrain is help performance
- review synthesis result (timing/power)

STAT/Timing Closure

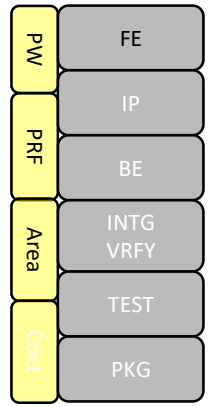
- Review violation timing path
- Sizing /remove cell to meet timing spec

DFT

MBIST => Self test Memory in the SOC.
SCAN => Check connectivity between different flops in the design
BSD => Test chip IO's interconnect.

KeyASIC

FE

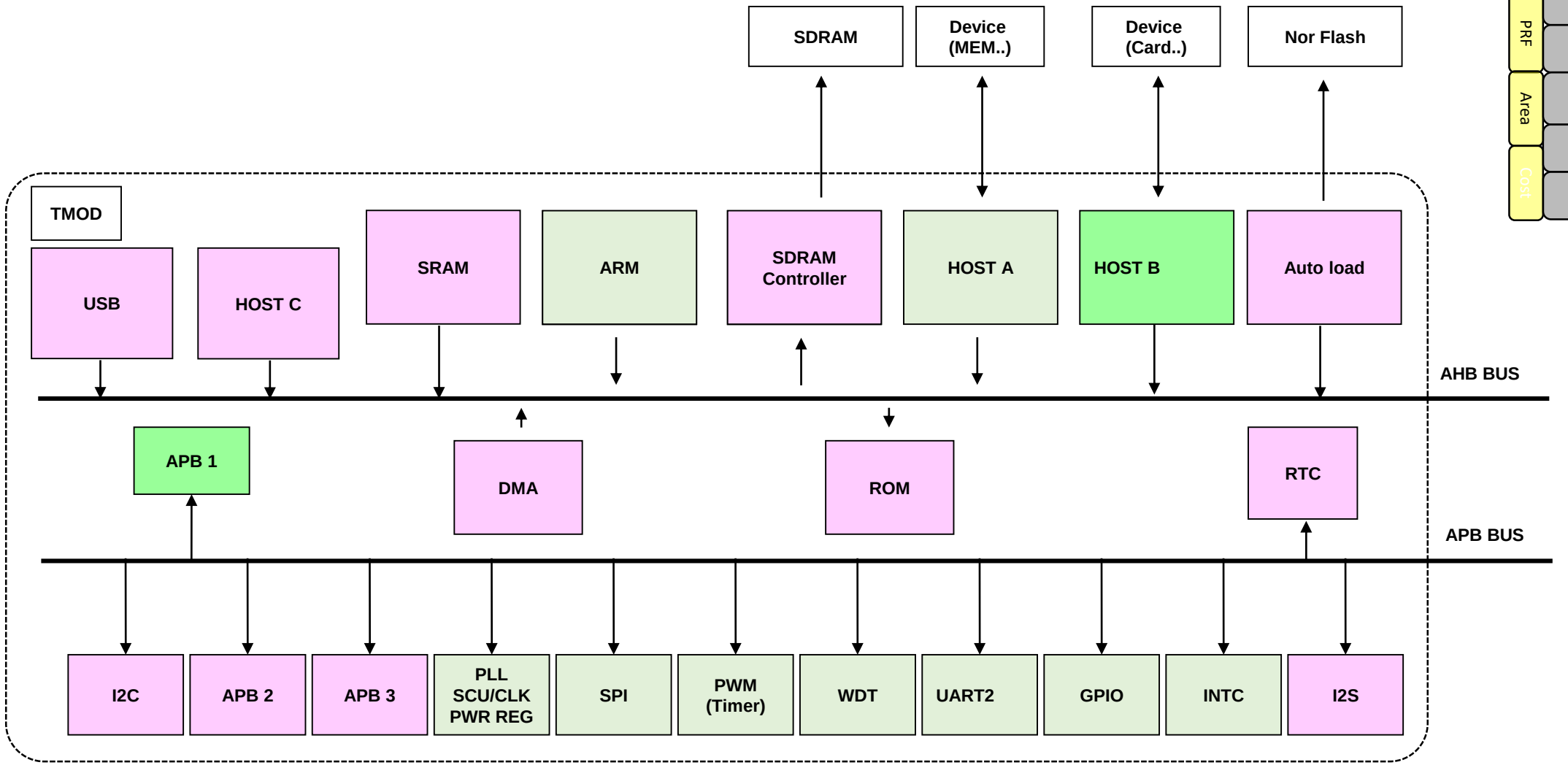


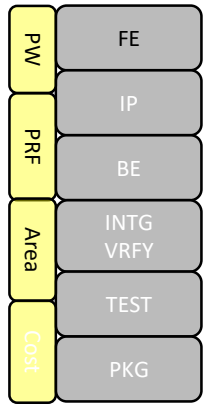
Some of the consideration

- SOC Arch
- Clock/Reset Arch
- Power Plan
- Memory usage

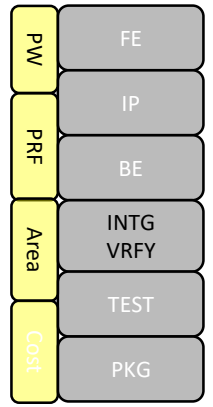
KeyASIC

Design Architecture

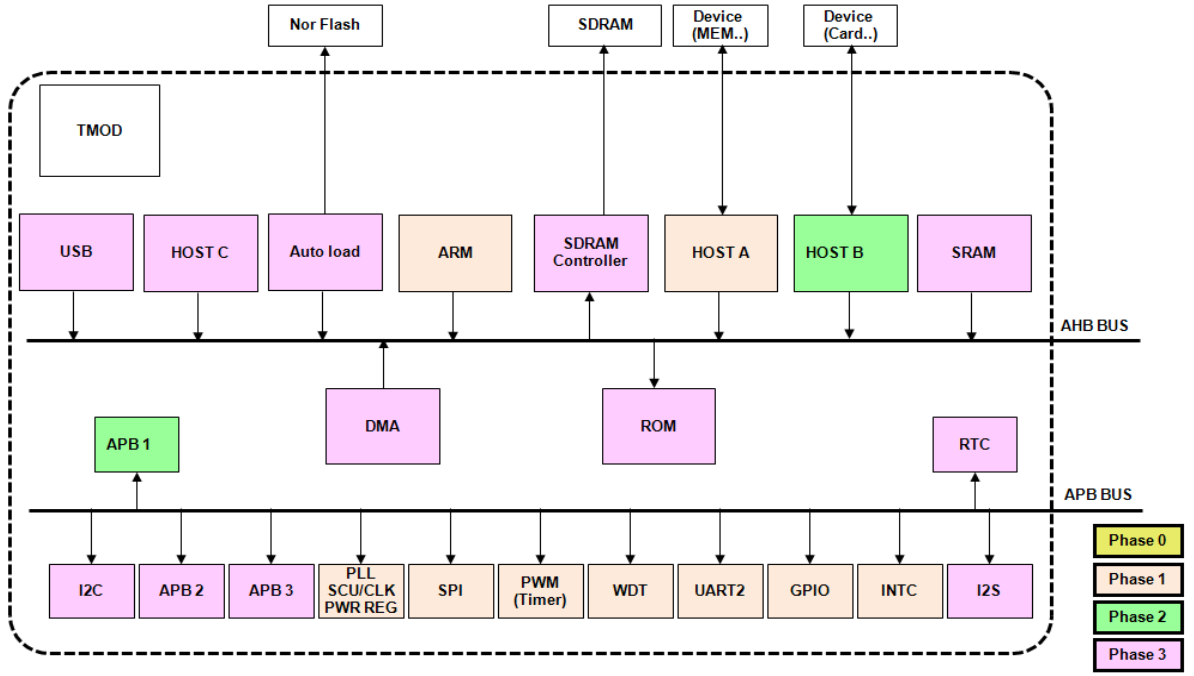




Scenario #1

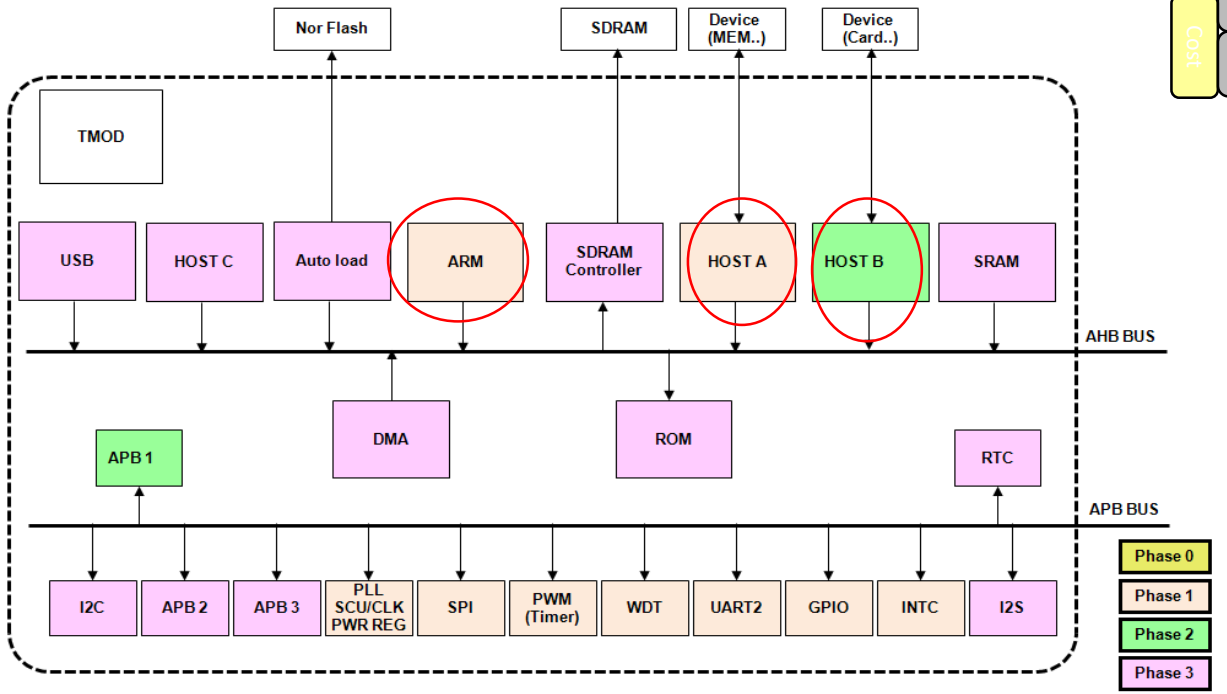


- Performance issue at Host C .
- Host C is the AHB Slave, It is need SW to control the DMA access from HOST C to SDRAM.
- After analysis with it. We find SW is need spend 2 time move data form HOST C to DMA . DMA -> SDRAM. This performance is not good.
- After Optimization this arch. We modify the HOST C to AHB Master. It could direct access data to SDRAM by himself. It could reduce a lot of access time.



Scenario #1.2

- Check MBIST is work
- EX: ARM/HOST A/HOAT B have MBIST inside
- confirm these module could work success in function mode.



KeyASIC

CLK / RST

PW
PRF
Area
Cost

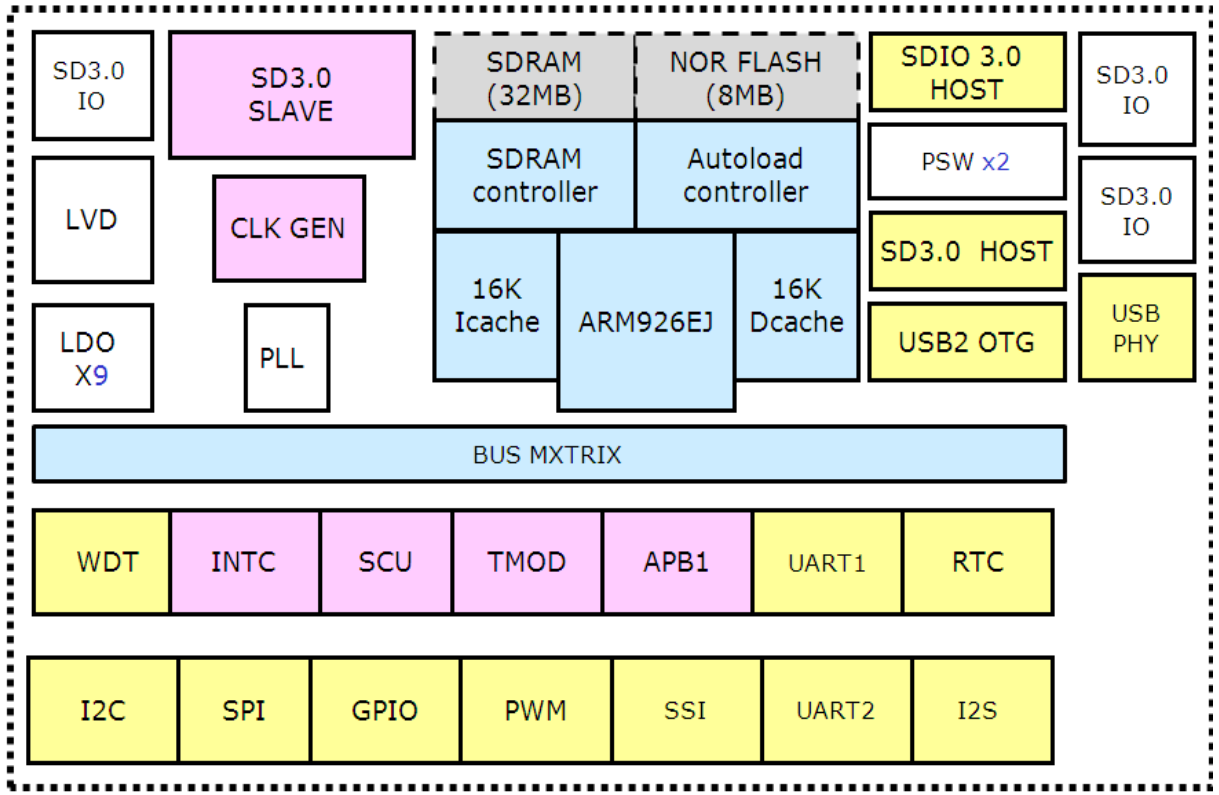
FE
IP
BE
INTG
VRFY
TEST
PKG

Some of the consideration

- Define Clock Arch for power save.
- Define Reset Arch

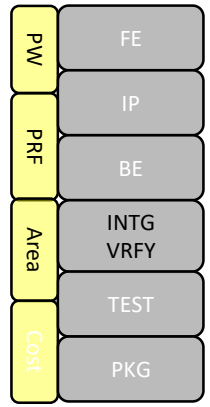
Scenario #2

- Review system power save plan
- Optimization RTL for Clock Gate
- Separate different operate mode for SW choose.



KeyASIC

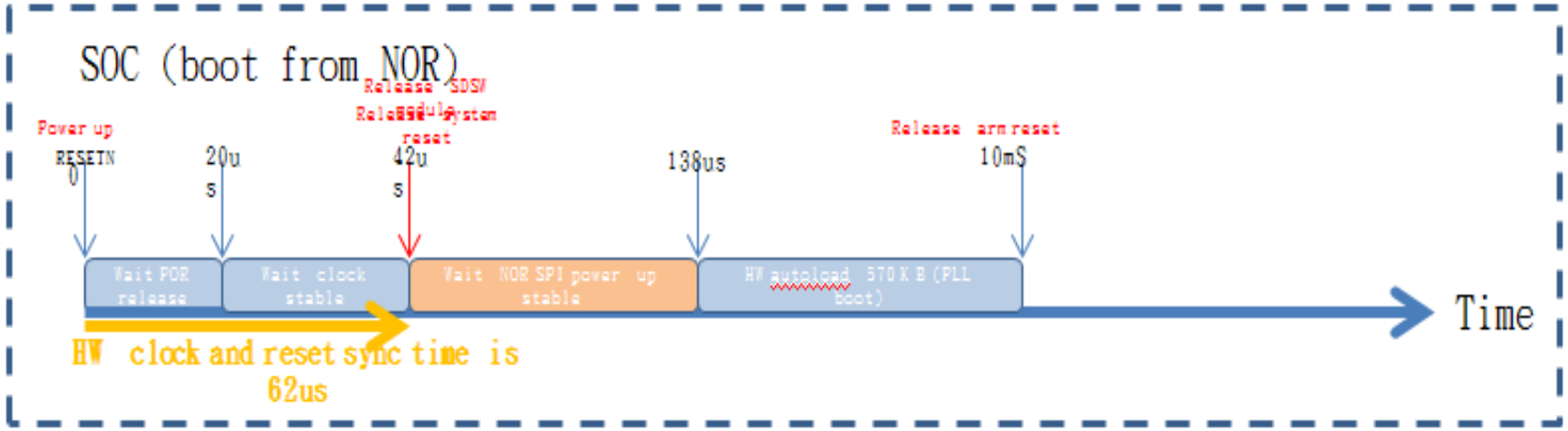
Boot Sequence



Things to consider in mind

- Define HW/SW Boot flow.
- Optimize Boot flow is meet timing/Power.
- Overall Boot time reduced

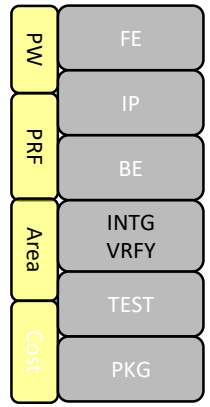
Scenario #3



- Check HW/SW Boot flow.
- Review boot plan with timing and power.
- Optimize HW Boot flow.
- Confirm Boot flow is suit real application

KeyASIC

Power Plan

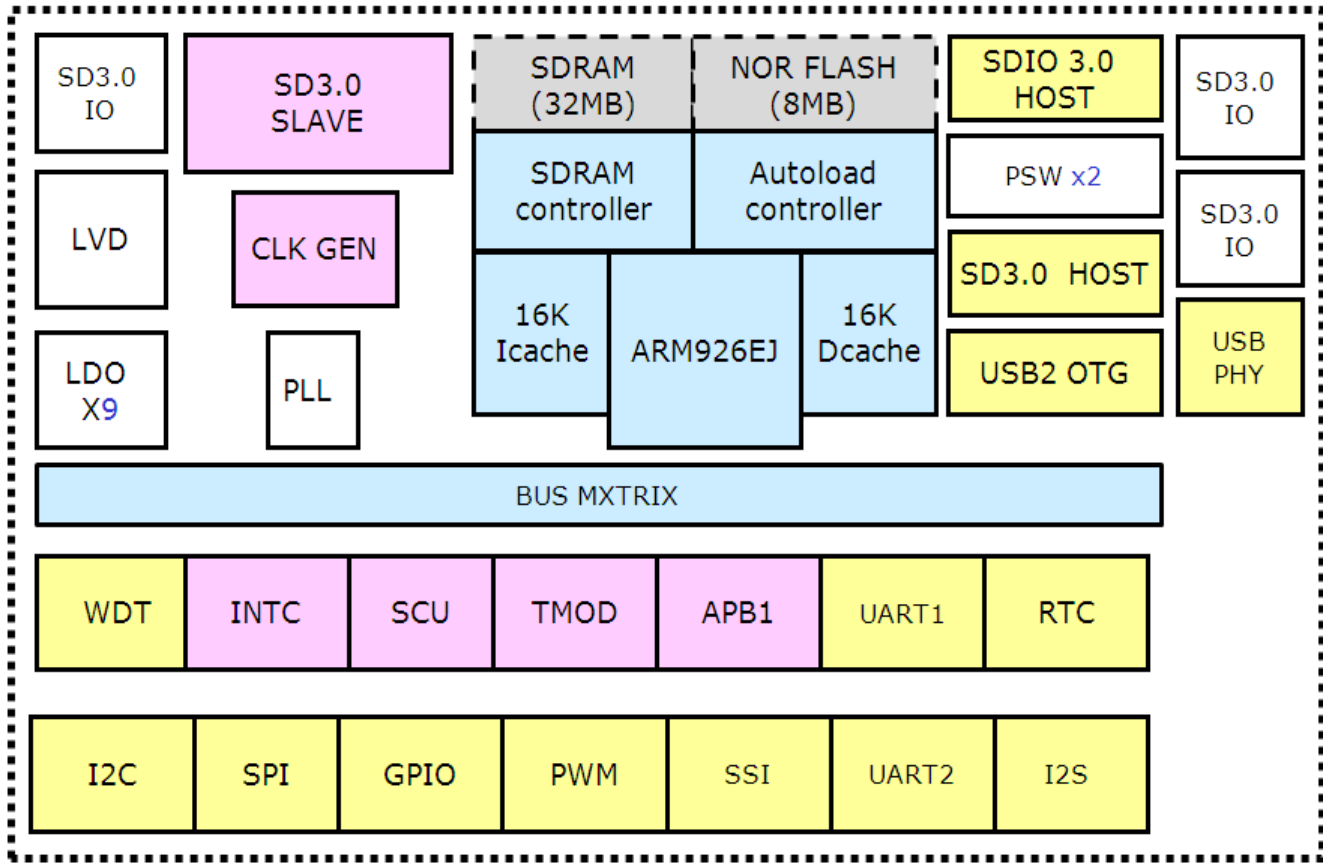


Design for Power

- Power saving plan
- Review IP/MEM usage

Scenario #3

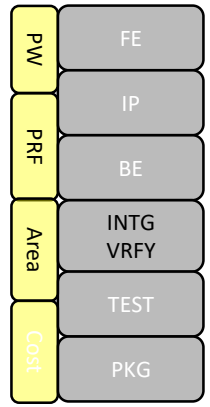
- Review IP (Memory/PLL/LDO/IP) usage.
- Check real application timing/power limit
- Optimization suit IP usage status.



PW
PRF
Area
Cost
FE
IP
BE
INTG VRFY
TEST
PKG

KeyASIC

PPA



Always think of how to improve PPA

KeyASIC

Summary

- PPAC as the key index to measure how good a chip is Besides having the right knowledge & skillset
- FE is the area that you should design-in & optimize PPA the most in overall design execution
- Execute your flow with disciplines, always check back against PPAC at any stages!

KeyASIC

Thank You