Discipline & Good Practise of the ASIC/SoC Design Methodology

March 2019

Moscow

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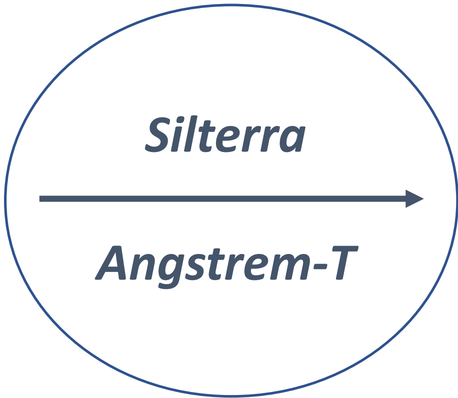
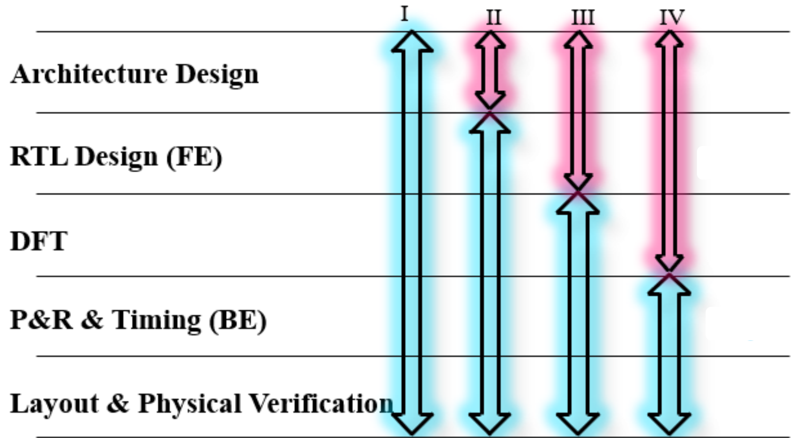
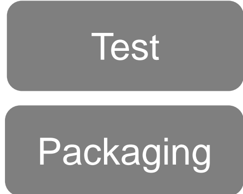
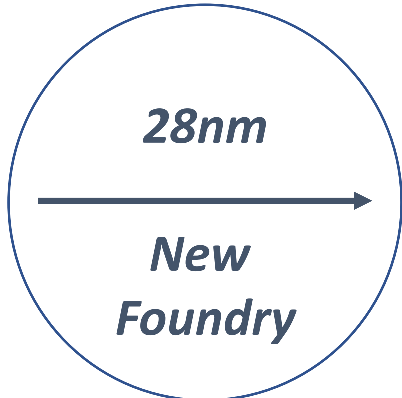
Capabilities

Customers









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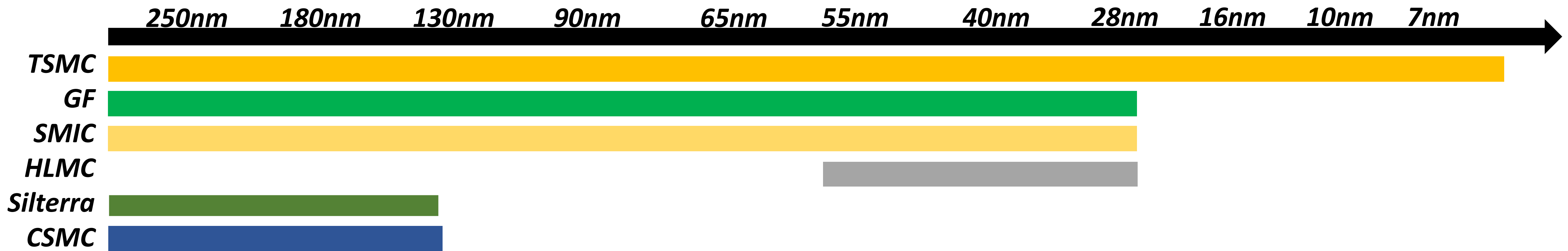

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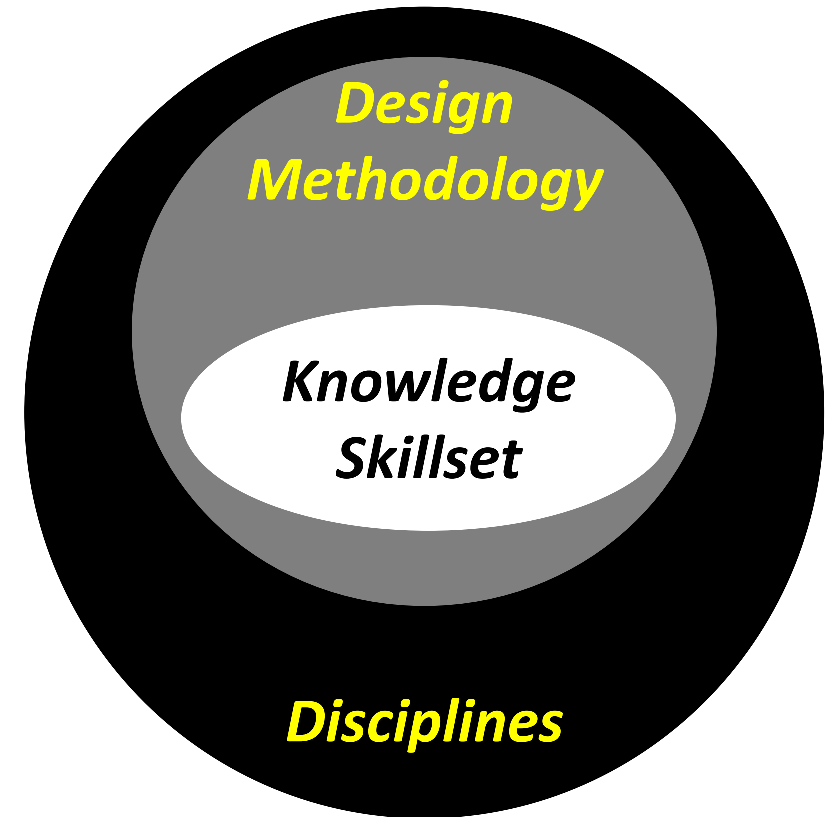
What else besides KNOWLEDGE?

What is needed in designing an ASIC/SoC?

- **Knowledge & skillset to design**
- **Establish competitive design methodology**
- **Discipline & Practice to execute/review (Attitude)**



Methodology: A System of Methods that connect expertise in different area

What are the criteria of a competitive chip design methodology?

Figure of Merit

There are at least **4 important parameters** to be considered in designing & commercializing ASIC/SoC:

POWER

PERFORMANCE

AREA

COST

Consist of various concerns that are very often unaddressed or overlooked during any stages!!!

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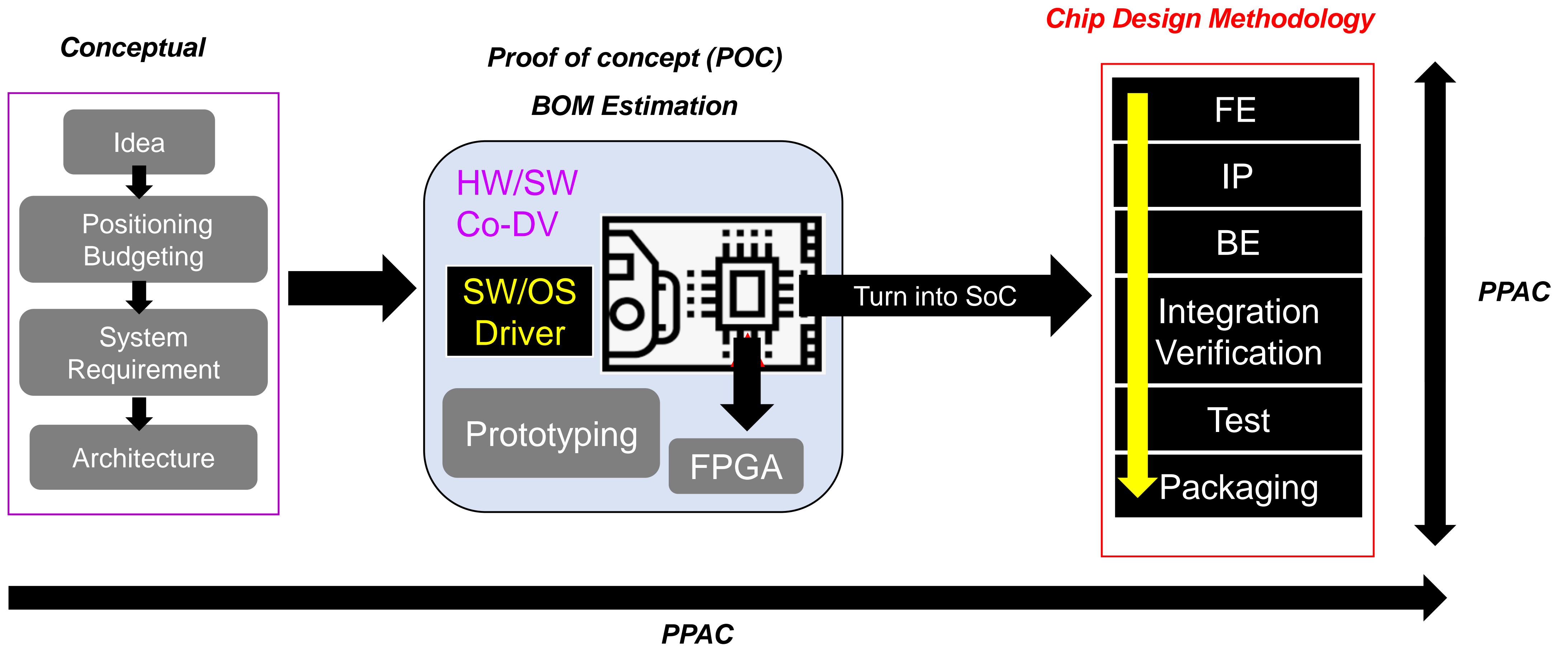
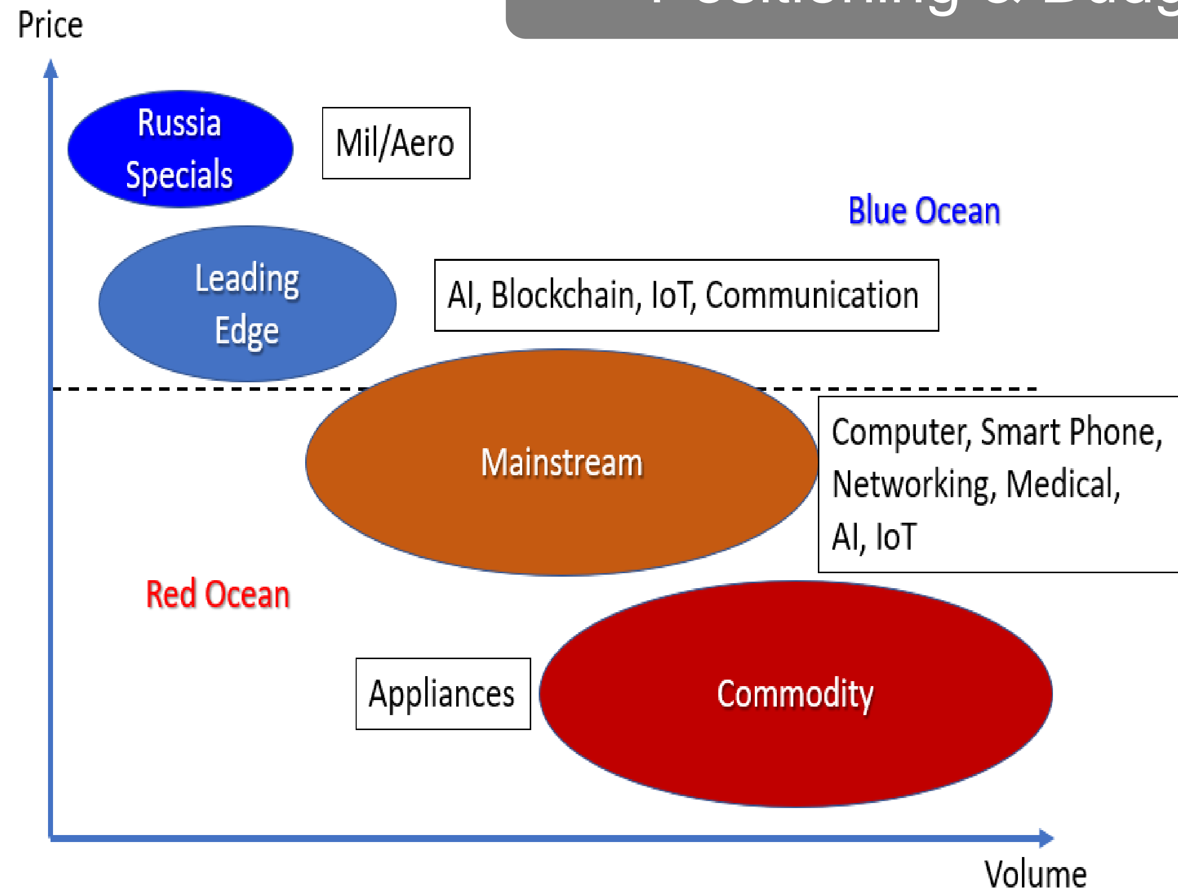
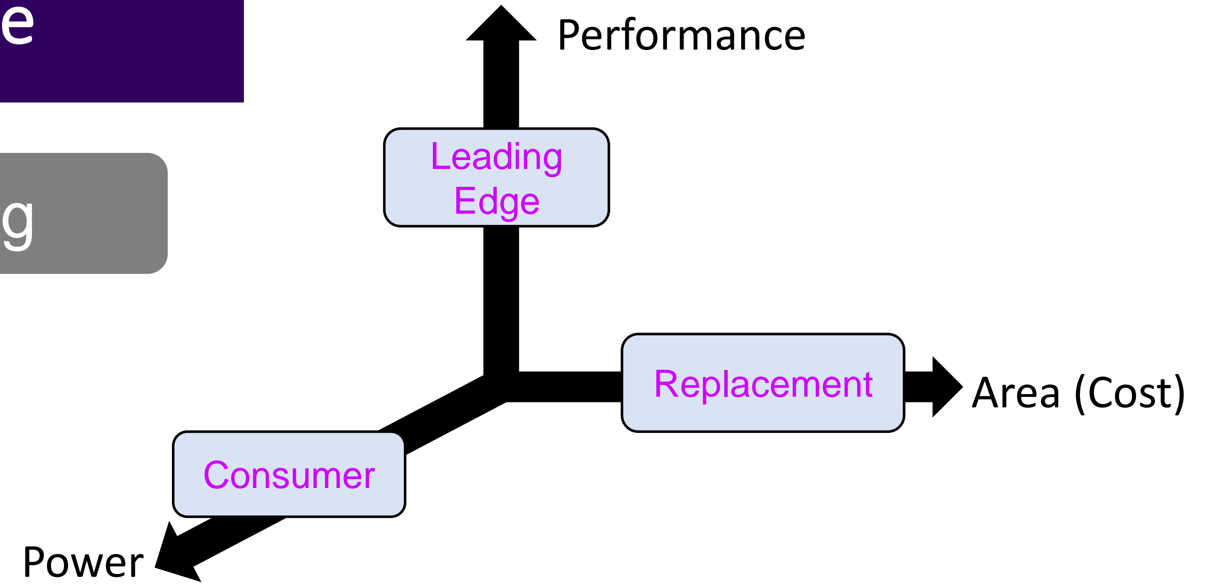
Complete Flow



PPAC at Conceptual Stage

Positioning & Budgeting





3 main chip unit cost:

- Die (area)
- Package (cost)
- Test (cost)

PPAC Profiling/Budgeting:

- Spec out targeted PPAC
- Knowing the traded-off
- Cost budgeting

(impact design, ex: package)

POC & HW/SW CO-DV

Shorten time-to-market → lower the cost

"pre-silicon validation of the embedded system"

- Accelerate SW OS drivers development
- Verify your HW(digital) the earliest
- Simplify HW/SW integration
- Increase real application test coverage

Reference: http://www.ccs.asia.edu.tw

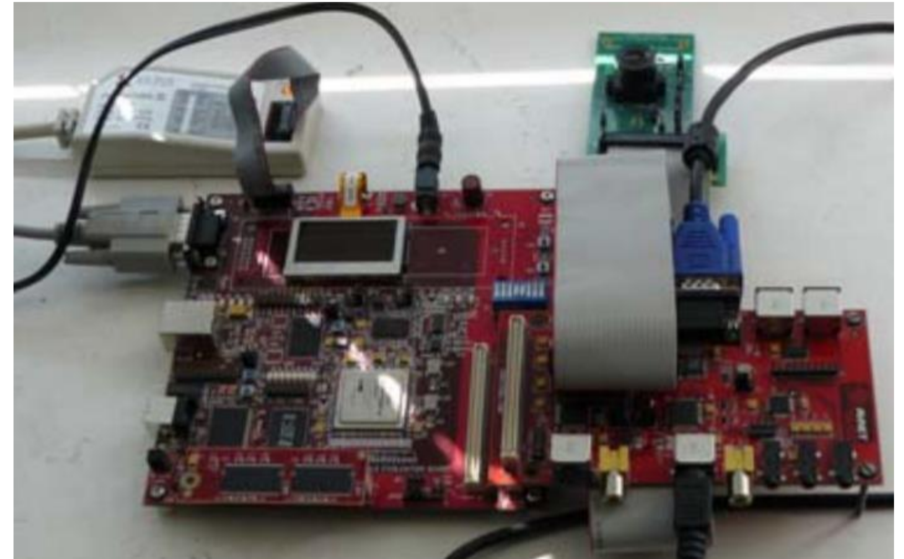
FPGA & Prototyping

Choose the right approach based on the complexity of your chip & the goal of prototyping….

1. Standalone FPGA for earliest proof of concept (mostly-digital-based IC)

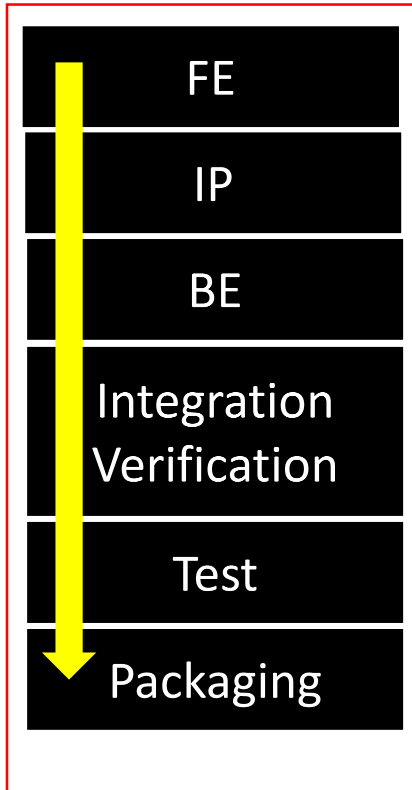
2. FPGA + custom daughters blocks to sign-off major application specific blocks & complex analog IP (Good for multi-chip module or SiP)

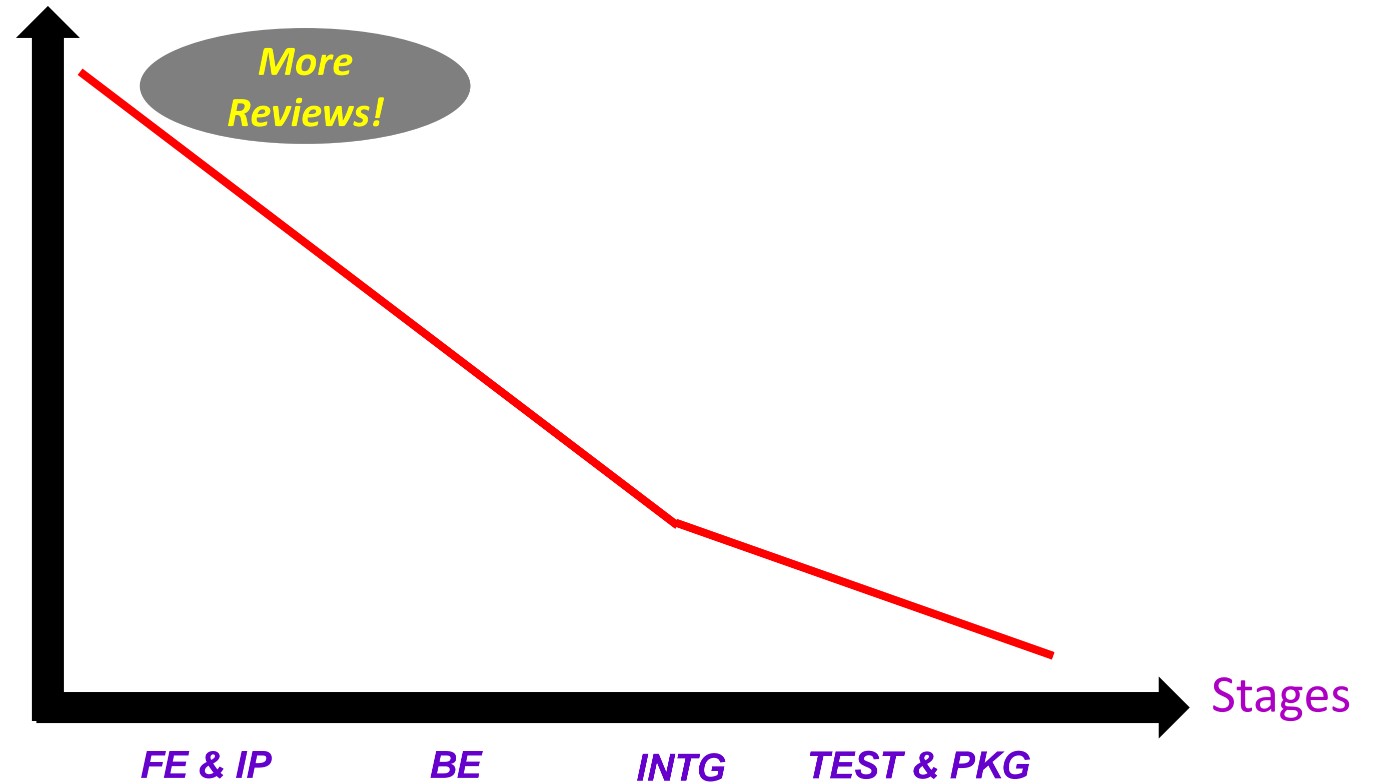
3. Full custom board to completely verify system (* HW/SW Co-DV)



Methodology & PPAC

Chip Design Methodology





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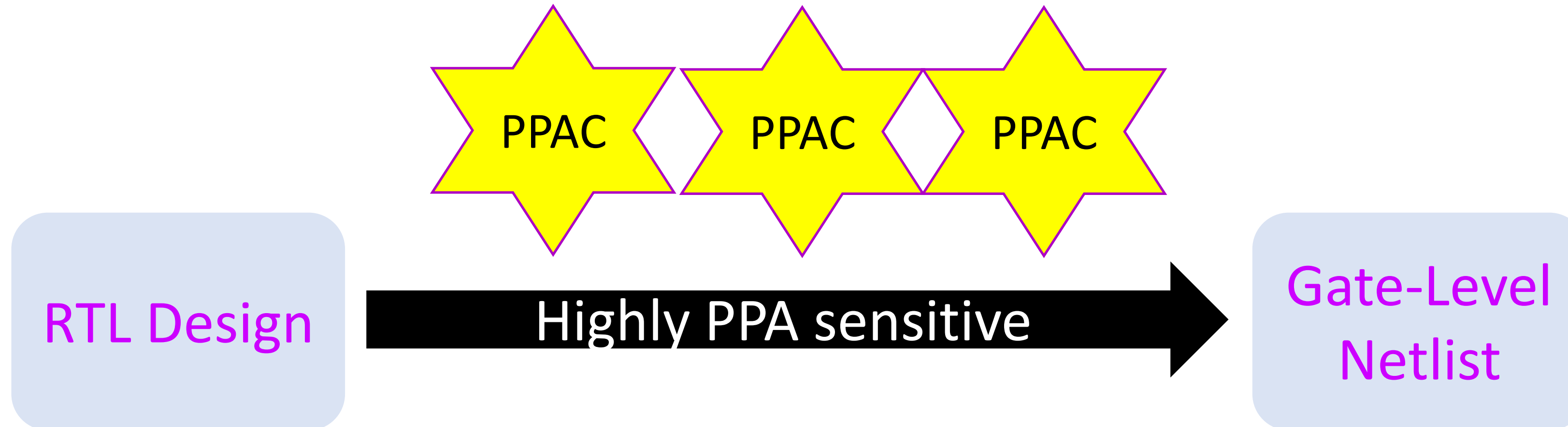
Front-End



- Functional Verification
- RTL optimization to reduce area
- SDC constraint-writing
- ULP flow UPF (Multi-V, DFVS)
- Synthesis as key PPA check-point
- Area-oriented .vs timing-oriented synthesis
- Pre-layout STA & PT-Power

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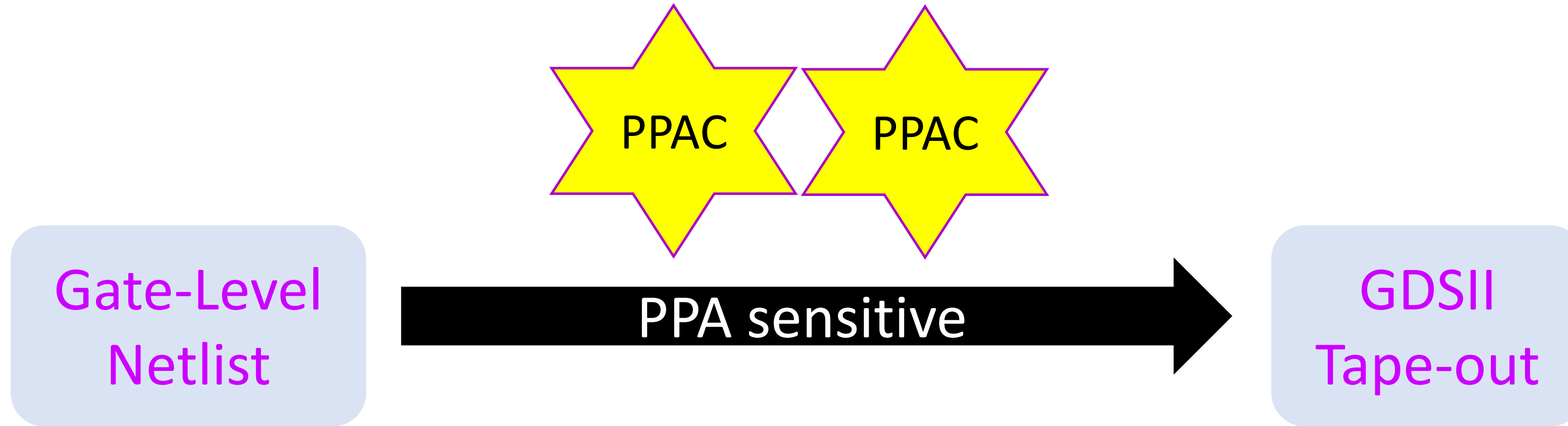
Back-End



- Physical Design (awareness-based P&R topologies)
- Do not give-in on performance deterioration during P&R
- Master advanced P&R tools & skillset
- ULP SoC segmentation and power routing (Multi-V, DFVS)
- MCMM to optimize design & meet most requirement
- Physical verification

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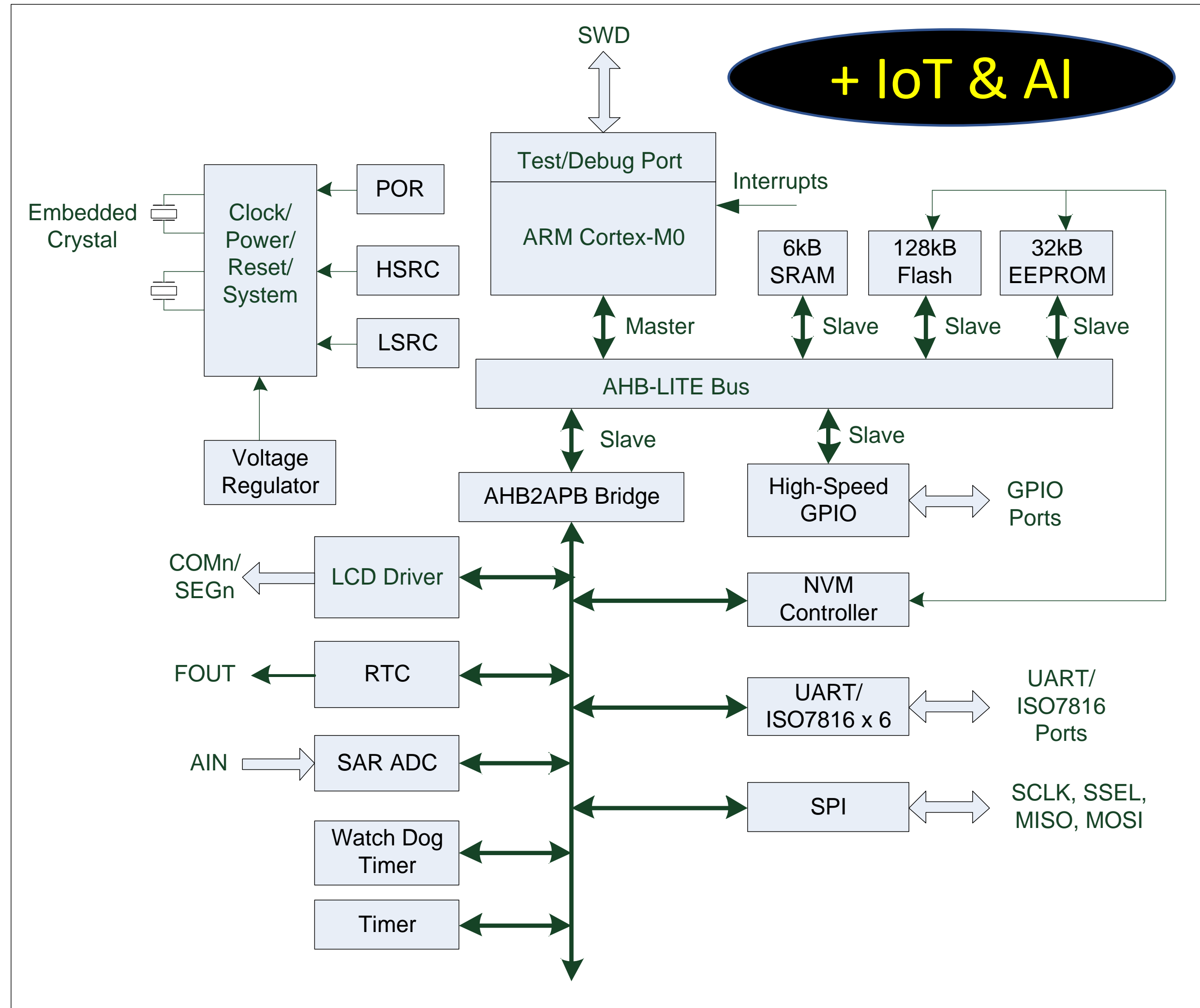
Integration & Verification

- Good integration ➔ bring you your targeted PPAC but no extra bonus
- Poor integration ➔ bring you worse PPAC
- Bus architecture, priority bus service (QoS), memory size, power saving mode, data path bottleneck and throughput optimization
- Verification is important to ensure your design function and meet PPA. It should be done at all levels.

SoC Building Blocks



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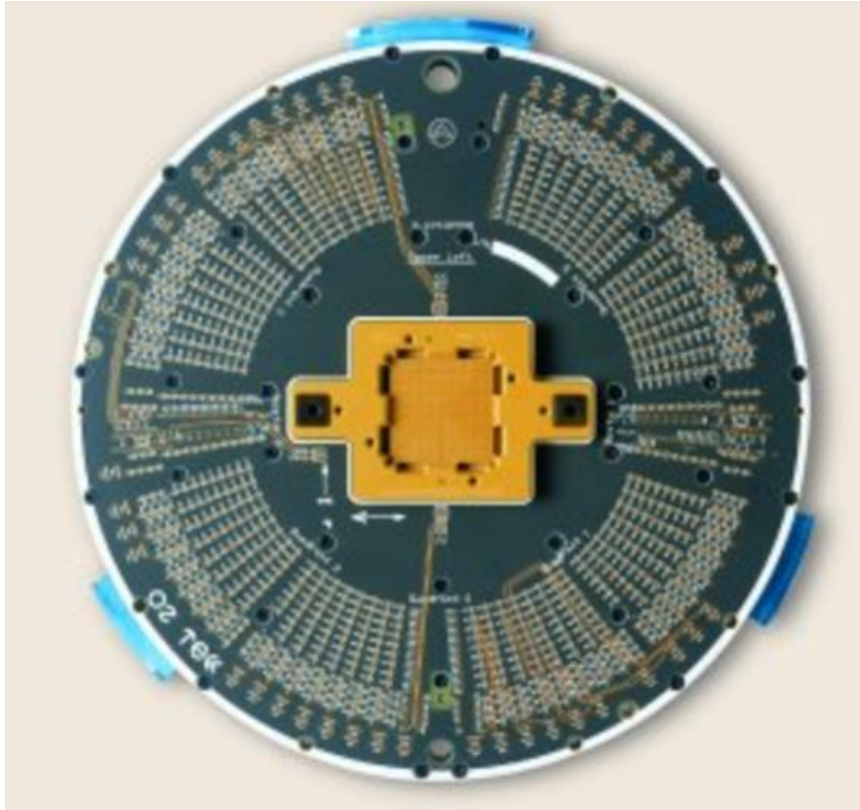
Testing & Packaging



- Package Selection

- at least 30% of total unit chip cost

- change chip design to meet the cost (PPAC budgeting)

- IC Testing

- Select the right tester for lower test-time & cost

- Reliability & Compatibility (often overlooked)

- Conduct test at the earliest as it may introduce unexpected design changes

Common mistakes: start test after few round of MPW tape-out

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Testing the Reliability

"Losses in the electronics industry have been estimated to range anywhere from half a billion dollars to $5 billion." – ESDA, 2017

- Cost a business in many different ways
- Total damages of a ruined devices
- Latent defects can have lasting costs tied to efficiency
- Crisis points causing your business to have to postpone product delivery.

Scenario

"An ASIC project was delayed for 6 months in production due to latch-up issues. Caused total loss of USD$400,000."

What is the design flow & disciplines?

- ESD/LU circuit design & layout
- I/O padring formation ESD/LU guideline
- Simulate & verify I/O pad-ring in term of ESD/LU

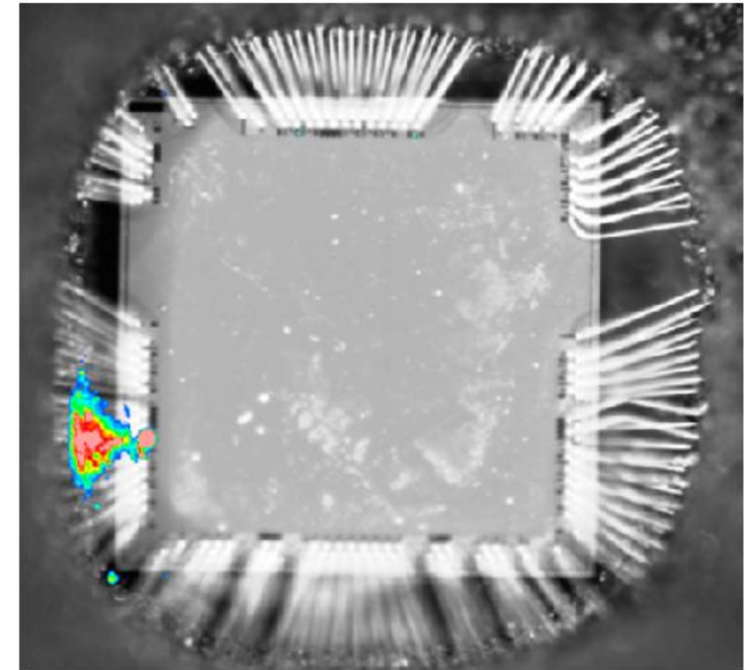
What could possibly went wrong?

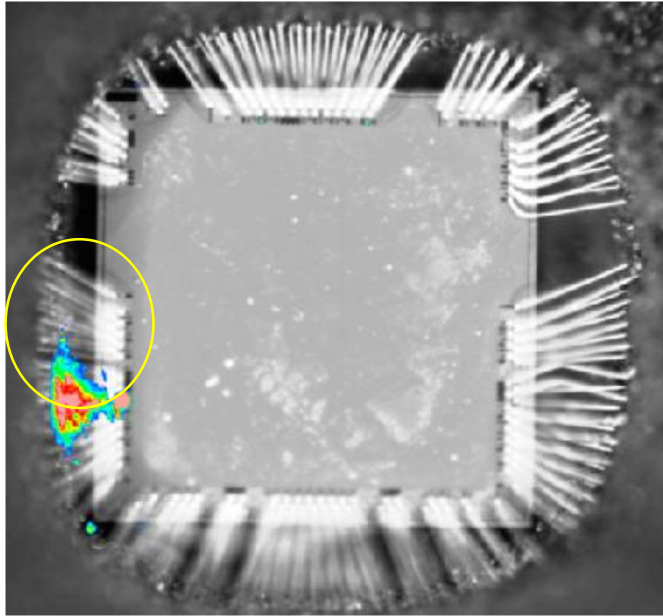
- Insufficient ESD design
- I/O design too compact, little spacing for LU
- Violate I/O padring guideline & lack of guard-ring
- Discrepancies with real application

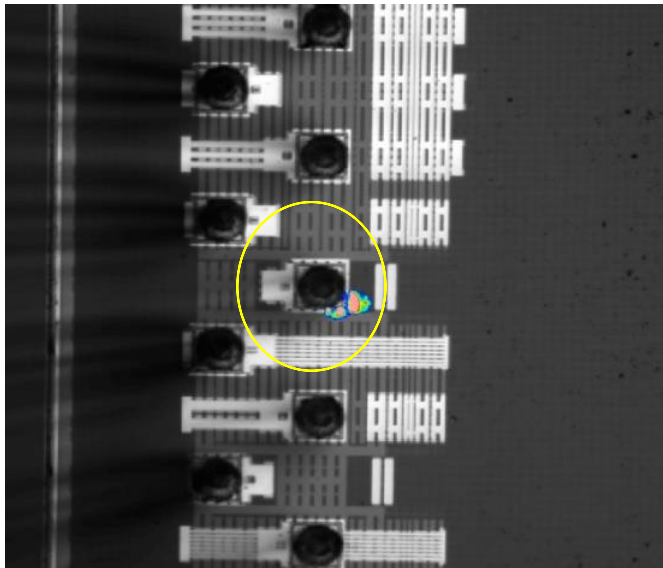
(ex: current consumption profile)

Pin 27 – PAD4 SST18 latched current >> 100mA

0.8X zoom







- I/O Layout violate LU spacing guideline
- I/O abutment did not follow the proper guideline

Did not follow the good I/O layout practise
Lack of methodology to verify (now some already built into DRC)
Lack of methodology to govern the formation of I/O padring

Summary

- PPAC as the key index to measure how good a chip is
- Besides having the right knowledge & skillset, a competitive design methodology is required
- Execute your flow with disciplines, always check back against PPAC at any stages!
- A chip design methodology outline is presented and will be covered in details in the coming sessions

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Thank You