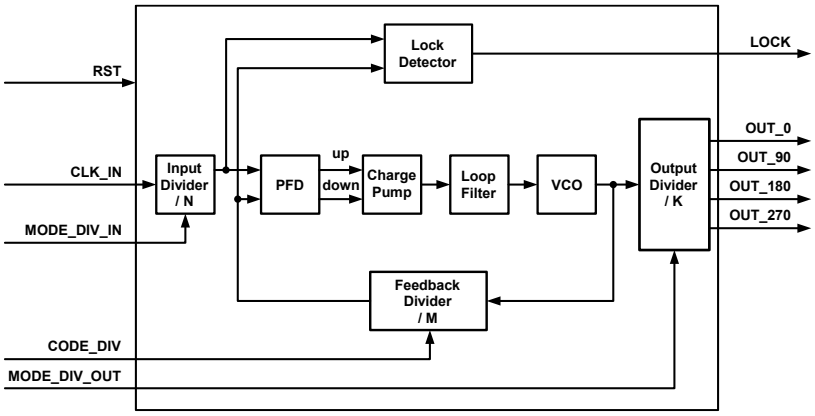
MALT-PLL

IP-Core. Phase-Locked Loop

Ред. 05.06.2026



The IP core is designed for synchronizing high-speed data transfers and generates four output clock signals, each of which is phase-shifted by 90° relative to the adjacent one (0°, 90°, 180°, 270°). The voltage-controlled oscillator (VCO) in the block operates in the frequency range from 933 MHz to 1600 MHz. The IP core is sensitive to interference from the power supply. The PLL assumes that the input signal is unipolar with an amplitude of the CMOS level and, therefore, cannot be connected directly to the crystal oscillator. Furthermore, since the PLL does not assume a direct connection, it does not have built-in electrostatic discharge protection devices, so the user must install them independently, even if the reference signal is a regular CMOS signal. Each time the configuration of the input divider or the feedback divider is changed, the lockout timer must be reset. The solution is designed for use in processors, radio transmitters and receivers for the purpose of tuning, modulation and demodulation, and ensuring synchronous data transmission.

Technical specifications

IP-Core type:	Physical (HARD IP)
IP-Core status:	Silicon-proven in 2023
Technology, nm:	28
Output frequency, MHz:	933-1600
Reference signal frequency, MHz:	100
Division factor, -:	1-64
Settling time, us:	10 (max)
Supply voltage, V:	0.9
Regulator voltage, V:	1.8
Duty cycle, %:	46-51
Absolute jitter, ps:	18 (1600 MHz) 22 (933 MHz)
Power dissipation, mW:	2.2
Macro area, mm^2:	0,0086
Delivery terms:	Ready for delivery

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Applications

- Conversion of a low-frequency reference signal into a high-frequency one for the operation of processors, microcontroller cores, data buses and high-speed logic;
- In specialized SoCs for synchronization of phases and frequencies of signals.
- Providing ultra-low sampling jitter for ADCs and DACs.
- Extraction of a reference frequency from radio waves containing phase noise and delays for receiving narrowband digital signals.

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