MALT-64G-ADC

IP-Core. Analog-to-Digital Converter

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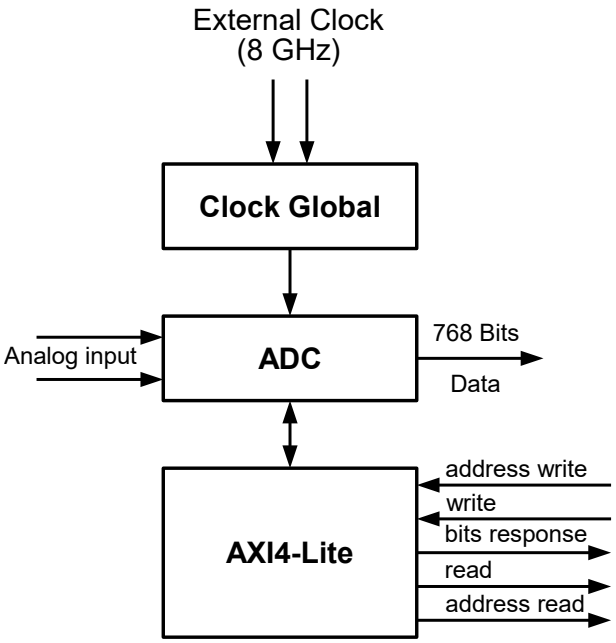

A high-speed RF ADC IP-block for direct digitization of wideband analog signals. The block is based on a SAR-architecture with time interleaving, the key element of which is the synchronization system and clock distribution between subchannels. To compensate for technological and operational variations in spectral characteristics, built-in algorithms for calibrating the zero offset, gain, and timing mismatches between channels are implemented. The digital portion of the block generates the output data stream and contains the AXI-Lite control interface, which is necessary for configuring operating modes, running built-in calibration procedures, and monitoring status. The solution is designed for use in high-speed receiving paths, coherent optics systems, measurement equipment, and scientific instruments.

Technical specifications

IP-Core type:	Physical (HARD IP)
IP-Core status:	Silicon-proven in 2023
Technology, nm:	28
Resolution, bits:	8
Sampling rate, GSa/s:	48–64
Architecture:	Time-interleaved SAR-ADC
Analog input bandwidth, GHz:	16
Supply voltage, V:	0,9 (nom.)
Power dissipation, mW:	600 (64 GSa/s)
Input configuration:	differential with DC coupling
Input resistance, Ohms:	50 (diff.)
Input capacity, fF:	30
Input peak-to-peak voltage (diff.), mVpp:	14-900
RMS aperture jitter, fs:	60
Macro area, mm^2:	0,6
Delivery terms:	Ready

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Applications

- Receive paths for coherent optical systems, including DP-QPSK and 16-QAM;
- Receive paths for data center interconnect (DCI) systems, including 100G/200G/800G Ethernet;
- High-speed oscilloscopes, digitizers, and other measurement equipment;
- Measurement and research systems, including quantum computing and spectroscopy;
- Specialized SoCs for real-time digital processing of high-frequency signals.